19-5646; Rev 0; 12/10

EVALUATION KIT AVAILABLE

HDCP Gigabit Multimedia Serial Link Serializer with LVDS System Interface

General Description

The MAX9265 gigabit multimedia serial link (GMSL) serializer features an LVDS system interface and high-bandwidth digital content protection (HDCP) encryption for content protection of DVD and Blu-ray™ video and audio data. The serializer pairs with any HDCP GMSL deserializer to form a digital serial link for the transmission of control data and HDCP-encrypted video and audio data. GMSL is an HDCP technology approved by Digital Content Protection (DCP), LLC.

The 3-channel mode serializes three lanes of LVDS data (21 bits), UART control signals, and three audio inputs. The 4-channel mode serializes four lanes of LVDS data (28 bits), UART control signals, three audio inputs, and auxiliary control inputs. The three audio inputs are for I²S audio, supporting a sampling frequency from 8kHz to 192kHz and a sample depth of 4 to 32 bits. The embedded control channel forms a full-duplex differential 9.6kbps to 1Mbps UART link between the serializer and deserializer. An electronic control unit (ECU), or microcontroller (µC), can be located on the serializer side of the link (typical for video display), on the deserializer side of the link (typical for image sensing), or on both sides. The control channel enables ECU/µC control of peripherals on the remote side, such as backlight control, touch screen, and perform HDCP-related operations.

The serial link signaling is AC-coupled CML with 8b/10b coding. For driving longer cables, the serializer has programmable driver pre/deemphasis, and for reduced EMI, has programmable spread spectrum on the serial output. The serial output meets ISO 10605 and IEC 61000-4-2 ESD standards.

The serializer operates with a 1.8V core supply, a 1.8V to 3.3V I/O supply, and a 3.3V LVDS supply. This device is available in a 48-pin TQFP package with an exposed pad and is specified over the -40°C to +105°C automotive temperature range.

Applications

High-Resolution Automotive Navigation

Rear-Seat Infotainment

Megapixel Camera Systems

Blu-ray is a trademark of Blu-ray Disc Association.

Features

- **Pairs with Any GMSL Deserializer**
- **HDCP Encryption Enable/Disable Programmable with the Control Channel**
- **Control Channel Handles All HDCP Protocol Transactions—Separate Control Bus Not Required**
- **HDCP Keys Preprogrammed in Secure Nonvolatile Memory**
- **2.5Gbps Payload Data Rate (3.125Gbps with Overhead)**
- **AC-Coupled Serial Link with 8b/10b Line Coding**
- **8.33MHz to 104MHz (3-Channel LVDS) or 6.25MHz to 78MHz (4-Channel LVDS) Pixel Clock**
- **4-Bit to 32-Bit Sample Depth, 8kHz to 192kHz I²S Audio Channel Supports High-Definition Audio**
- **Embedded Half-/Full-Duplex Bidirectional Control Channel**
  - **Base Mode: 9.6kbps to 1Mbps**
  - **Bypass Mode: 9.6kbps to 1Mbps**
- **Two 3-Level Inputs Support 9 Slave Addresses**
- **Interrupt Supports Touch-Screen Displays**
- **Remote-End I²C Master for Peripherals**
- **Programmable Pre/Deemphasis**
- **Programmable Spread Spectrum on the Serial Link and Deserializer Outputs Reduce EMI**
- **Auto Data-Rate Detection Allows "On-The-Fly" Data-Rate Change**
- **Bypassable PLL on LVDS Clock Input for Jitter Attenuation**
- **Built-In PRBS Generator for BER Testing of the Serial Link**
- **Fault Detection of Serial Link Shorted Together, to Ground, to Battery, or Open**
- **ISO 10605 and IEC 61000-4-2 ESD Tolerance**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9265GCM/V+	-40°C to +105°C	48 TQFP-EP*
MAX9265GCM/V+T	-40°C to +105°C	48 TQFP-EP*

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
T = Tape and reel.

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ABSOLUTE MAXIMUM RATINGS

AVDD to AGND .....-0.5V to +1.9V
DVDD to GND .....-0.5V to +1.9V
IOVDD to GND .....-0.5V to +3.9V
LVDSVDD to AGND.....-0.5V to +3.9V
Any Ground to Any Ground .....-0.5V to +0.5V
RXIN__, RXCLKIN_ to AGND .....-0.5V to +3.9V
OUT+, OUT- to AGND .....-0.5V to +1.9V
LMN_ to AGND (15mA current limit).....-0.5V to +3.9V
All Other Pins to GND .....-0.5V to (VIOVDD + 0.5V)
Continuous Power Dissipation (T_A = +70°C)
48-Lead TQFP (derate 36.2mW/°C above +70°C)..2898.6mW

Junction-to-Case Thermal Resistance (θ_{JC}) (Note 1)
48-Lead TQFP.....2°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1)
48-Lead TQFP.....27.6°C/W
Operating Temperature Range..... -40°C to +105°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, $V_{LVDSVDD}$ = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (SD/CNTL0, SCK, WS, CNTL1, CNTL2, SSEN, DRS, BWS, $\overline{PWDN}$, CDS, MS, $\overline{AUTOS}$)							
High-Level Input Voltage	V_{IH1}	$\overline{PWDN}$, SSEN, BWS, DRS, MS, CDS, $\overline{AUTOS}$		0.65 x V_{IOVDD}			V
		SD/CNTL0, SCK, WS, CNTL_		0.7 x V_{IOVDD}			
Low-Level Input Voltage	V_{IL1}					0.35 x V_{IOVDD}	V
Input Current	I_{IN1}	V_{IN} = 0 to V_{IOVDD}		-10		+10	µA
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA				-1.5	V
SINGLE-ENDED OUTPUT (INT)							
High-Level Output Voltage	V_{OH1}	I_{OUT} = -2mA		V_{IOVDD} - 0.2			V
Low-Level Output Voltage	V_{OL1}	I_{OUT} = 2mA				0.2	V
Output Short-Circuit Current	I_{OS}	V_O = V_{GND}	V_{IOVDD} = 3.0V to 3.6V	16	35	64	mA
			V_{IOVDD} = 1.7V to 1.9V	3	12	21	
I²C/UART, I/O, AND OPEN-DRAIN OUTPUTS (RX/SDA, TX/SCL, $\overline{LFLT}$)							
High-Level Input Voltage	V_{IH2}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL2}					0.3 x V_{IOVDD}	V
Input Current	I_{IN2}	V_{IN} = 0 to V_{IOVDD} (Note 2)		-110		+5	µA
Low-Level Output Voltage	V_{OL2}	I_{OUT} = 3mA	V_{IOVDD} = 1.7V to 1.9V			0.4	V
			V_{IOVDD} = 3.0V to 3.6V			0.3	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, $V_{LVDSVDD}$ = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIFFERENTIAL OUTPUTS (OUT+, OUT-)						
Differential Output Voltage	V_{OD}	Preemphasis off (Figure 1)	300	400	500	mV
		3.3dB preemphasis setting (Figure 2)	350		610	
		3.3dB deemphasis setting (Figure 2)	240		425	
Change in V_{OD} Between Complementary Output States	ΔV_{OD}				15	mV
Output Offset Voltage (V_{OUT+} + V_{OUT-})/2 = V_{OS}	V_{OS}	Preemphasis off	1.1	1.4	1.56	V
Change in V_{OS} Between Complementary Output States	ΔV_{OS}				15	mV
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V	-60			mA
		V_{OUT+} or V_{OUT-} = 1.9V			25	
Magnitude of Differential Output Short-Circuit Current	I_{OSD}	V_{OD} = 0V			25	mA
Output Termination Resistance (Internal)	R_O	From OUT+, OUT- to V_{AVDD}	45	54	63	Ω
REVERSE CONTROL-CHANNEL RECEIVER (OUT+, OUT-)						
High Switching Threshold	V_{CHR}				27	mV
Low Switching Threshold	V_{CLR}		-27			mV
LINE-FAULT-DETECTION INPUTS (LMN0, LMN1)						
Short-to-GND Threshold	V_{TG}	Figure 3			0.3	V
Normal Thresholds	V_{TN}	Figure 3	0.57		1.07	V
Open Thresholds	V_{TO}	Figure 3	1.45		V_{IO} + 60mV	V
Open Input Voltage	V_{IO}	Figure 3	1.47		1.75	V
Short-to-Battery Threshold	V_{TE}	Figure 3	2.47			V
THREE-LEVEL LOGIC INPUTS (ADD0, ADD1)						
High-Level Input Voltage	V_{IH}		0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{IOVDD}	V
Mid-Level Input Current	I_{INM}	Unconnected or connected to a driver with output in high-impedance state (Note 3)	-10		+10	µA
Input Current	I_{IN}		-150		+150	µA
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA			-1.5	V

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DC ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, $V_{LVDSVDD}$ = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LVDS INPUTS (RXIN_+/-, RXCLKIN_)							
Differential Input High Threshold	V_{TH}					50	mV
Differential Input Low Threshold	V_{TL}			-50			mV
Input Differential Termination Resistance	R_{TERM}			85	110	135	Ω
Input Current	I_{IN+}, I_{IN-}	$\overline{PWDN}$ = high or low, IN+ and IN- are shorted		-25		+25	µA
Power-Off Input Current	I_{IN0+}, I_{IN0-}	V_{AVDD} = V_{DVDD} = V_{IOVDD} = 0V		-40		+40	µA
POWER SUPPLY							
Worst-Case Supply Current (Figure 4)	I_{WCS}	HDCP enabled, BWS = low	$f_{RXCLKIN\_}$ = 16.6MHz		137	178	mA
			$f_{RXCLKIN\_}$ = 33.3MHz		146	186	
			$f_{RXCLKIN\_}$ = 66.6MHz		166	206	
			$f_{RXCLKIN\_}$ = 104MHz		195	242	
Sleep Mode Supply Current	I_{CCS}	LVDS inputs are not driven			95	225	µA
Power-Down Supply Current	I_{CCZ}	$\overline{PWDN}$ = GND, LVDS inputs are not driven			60	180	µA
ESD PROTECTION							
OUT+, OUT-	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF (Note 4)		±8			kV
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF (Note 5)	Contact discharge	±10			
			Air discharge	±12			
		ISO 10605, R_D = 2kΩ, C_S = 330pF (Note 5)	Contact discharge	±10			
			Air discharge	±20			
RXIN_+, RXIN_-, RXCLKIN+, RXCLKIN-	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF (Note 4)		±8			kV
All Other Pins	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF (Note 4)		±3.5			kV

AC ELECTRICAL CHARACTERISTICS

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, $V_{LVDSVDD}$ = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Differential input voltage $|V_{ID}|$ = 0.15V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CLOCK INPUTS (RXCLKIN_)							
Clock Frequency	$f_{RXCLKIN\_}$	BWS = GND, V_{DRS} = V_{IOVDD}		8.33		16.66	MHz
		BWS = GND, DRS = GND		16.66		104	
		V_{BWS} = V_{IOVDD}, V_{DRS} = V_{IOVDD}		6.25		12.5	
		V_{BWS} = V_{IOVDD}, DRS = GND		12.5		78	
I²C/UART PORT TIMING							
I²C/UART Bit Rate				9.6		1000	kbps
Output Rise Time	t_R	30% to 70%, C_L = 10pF to 100pF, 1kΩ pullup to V_{IOVDD}		20		150	ns
Output Fall Time	t_F	70% to 30%, C_L = 10pF to 100pF, 1kΩ pullup to V_{IOVDD}		20		150	ns
Input Setup Time	t_{SET}	I²C only (Figure 5, Note 6)		100			ns
Input Hold Time	t_{HOLD}	I²C only (Figure 5, Note 6)		0			ns
SWITCHING CHARACTERISTICS							
Differential Output Rise/Fall Time	t_R, t_F	20% to 80%, V_{OD} ≥ 400mV, R_L = 100Ω, serial bit rate = 3.125Gbps (Note 6)			90	150	ps
Total Serial Output Jitter	t_{TSOJ1}	3.125Gbps PRBS signal, measured at V_{OD} = 0V differential, preemphasis disabled (Figure 6)			0.25		UI
Deterministic Serial Output Jitter	t_{DSOJ2}	3.125Gbps PRBS signal			0.15		UI
CNTL_ Input Setup Time	t_{SET}	CNTL_ (Figure 7) (Note 6)		3			ns
CNTL_ Input Hold Time	t_{HOLD}	CNTL_ (Figure 7) (Note 6)		1.5			ns
RXIN__ Skew Margin	t_{RSKM}	Figure 8 (Note 6)		0.3			UI
Serializer Delay (Notes 6, 7)	t_{SD}	(Figure 9)	Spread spectrum enabled			2950	Bits
			Spread spectrum disabled			550	
Link Start Time	t_{LOCK}	(Figure 10)				3.5	ms
Power-Up Time	t_{PU}	(Figure 11)				6	ms
I²S INPUT TIMING							
WS Frequency	f_{WS}	See Table 4		8		192	kHz
Sample Word Length	n_{WS}	See Table 4		4		32	Bits
SCK Frequency	f_{SCK}	f_{SCK} = f_{WS} x n_{WS} x 2		(8 x 4) x 2		(192 x 32) x 2	kHz

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AC ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, $V_{LVDSVDD}$ = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Differential input voltage $|V_{ID}|$ = 0.15V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCK Clock High Time	t_{HC}	$V_{SCK} \geq V_{IH}$, $t_{SCK} = 1/f_{SCK}$ (Note 6)	0.35 t_{SCK}			ns
SCK Clock Low Time	t_{LC}	$V_{SCK} \leq V_{IL}$, $t_{SCK} = 1/f_{SCK}$ (Note 6)	0.35 t_{SCK}			ns
SD, WS Setup Time	t_{SET}	(Figure 12, Note 6)	2			ns
SD, WS Hold Time	t_{HOLD}	(Figure 12, Note 6)	2			ns

Note 2: Minimum I_{IN} due to voltage drop across the internal pullup resistor.

Note 3: To provide a mid level, leave the input unconnected, or, if driven, put driver in high impedance. High-impedance leakage current must be less than ±10µA.

Note 4: Tested terminal to all grounds.

Note 5: Tested terminal to AGND.

Note 6: Guaranteed by design and not production tested.

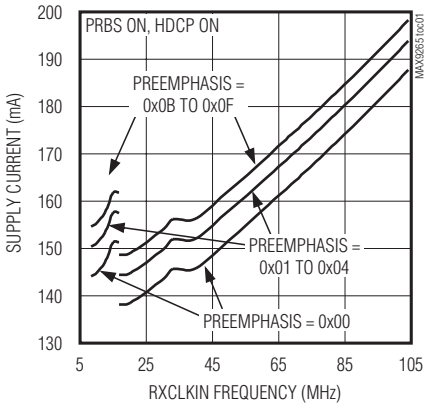
Note 7: Measured in CML bit times. Bit time = 1/(30 x $f_{RXCLKIN}$) for BWS = GND. Bit time = 1/(40 x $f_{RXCLKIN}$) for V_{BWS} = V_{IOVDD}.

HDCP Gigabit Multimedia Serial Link Serializer with LVDS System Interface

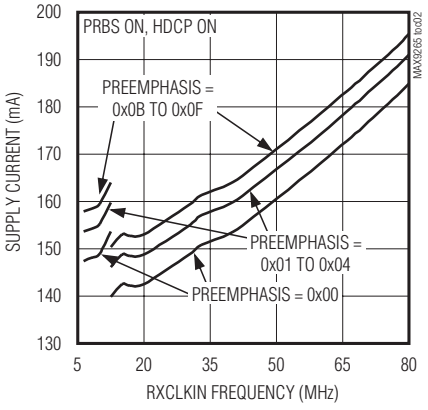
Typical Operating Characteristics

(V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C, unless otherwise noted.)

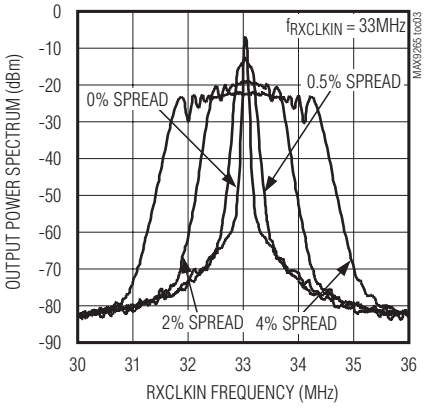
SUPPLY CURRENT vs. RXCLKIN_ FREQUENCY (24-BIT MODE)



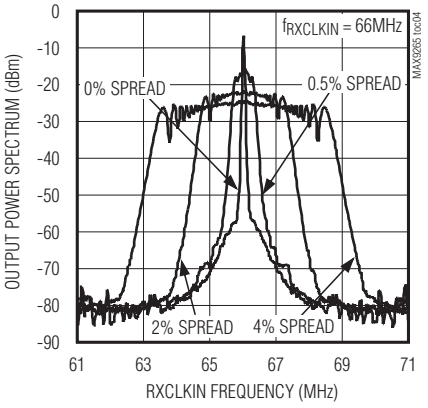
SUPPLY CURRENT vs. RXCLKIN_ FREQUENCY (32-BIT MODE)



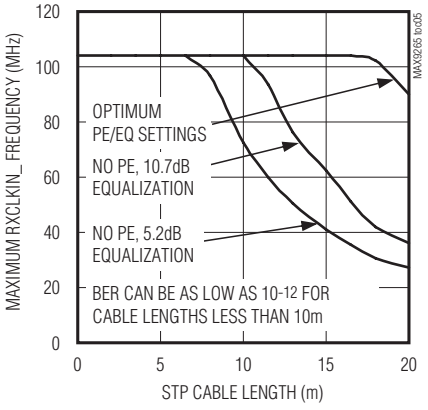
OUTPUT POWER SPECTRUM vs. RXCLKIN_ FREQUENCY (VARIOUS SPREAD)



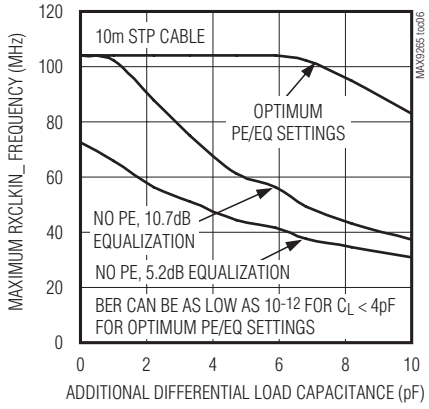
OUTPUT POWER SPECTRUM vs. RXCLKIN_ FREQUENCY (VARIOUS SPREAD)



MAXIMUM RXCLKIN_ FREQUENCY vs. STP CABLE LENGTH (BER < 10-9)

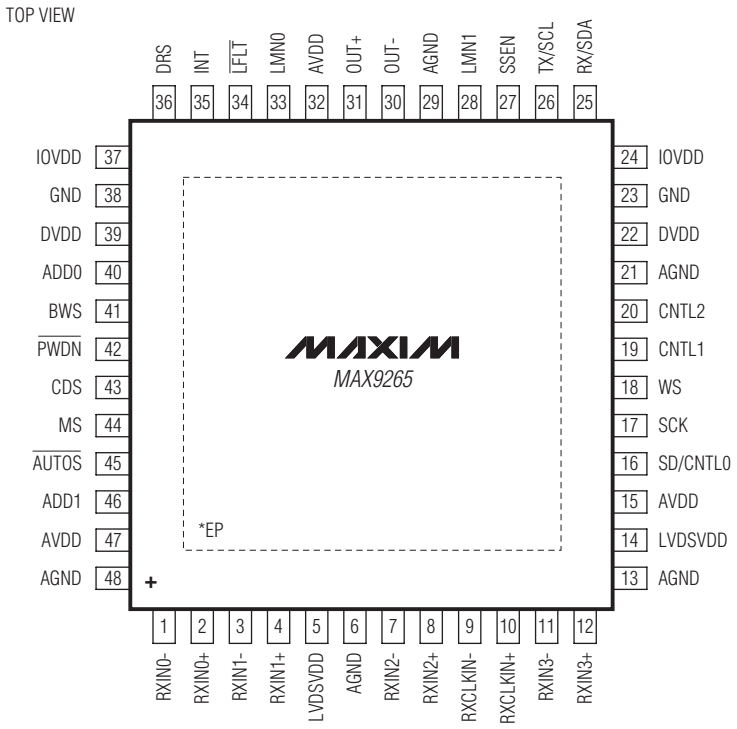


MAXIMUM RXCLKIN_ FREQUENCY vs. ADDITIONAL DIFFERENTIAL C_L (BER < 10-9)



HDCP Gigabit Multimedia Serial Link Serializer with LVDS System Interface

Pin Configuration



TQFP

*CONNECT EXPOSED PAD TO AGND

Pin Description

PIN	NAME	FUNCTION
1	RXIN0-	Differential LVDS Data Input 0-
2	RXIN0+	Differential LVDS Data Input 0+
3	RXIN1-	Differential LVDS Data Input 1-
4	RXIN1+	Differential LVDS Data Input 1+
5, 14	LVDSVDD	3.3V LVDS Power Supply. Bypass LVDSVDD to AGND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to LVDSVDD.
6, 13, 21, 29, 48	AGND	Analog Ground
7	RXIN2-	Differential LVDS Data Input 2-
8	RXIN2+	Differential LVDS Data Input 2+
9, 10	RXCLKIN-, RXCLKIN+	LVDS Input for the LVDS Clock
11	RXIN3-	Differential LVDS Data Input 3-. RXIN3- is not available in 3-channel mode. To use RXIN3-, drive BWS high (4-channel mode) (see Table 3).

Pin Description (continued)

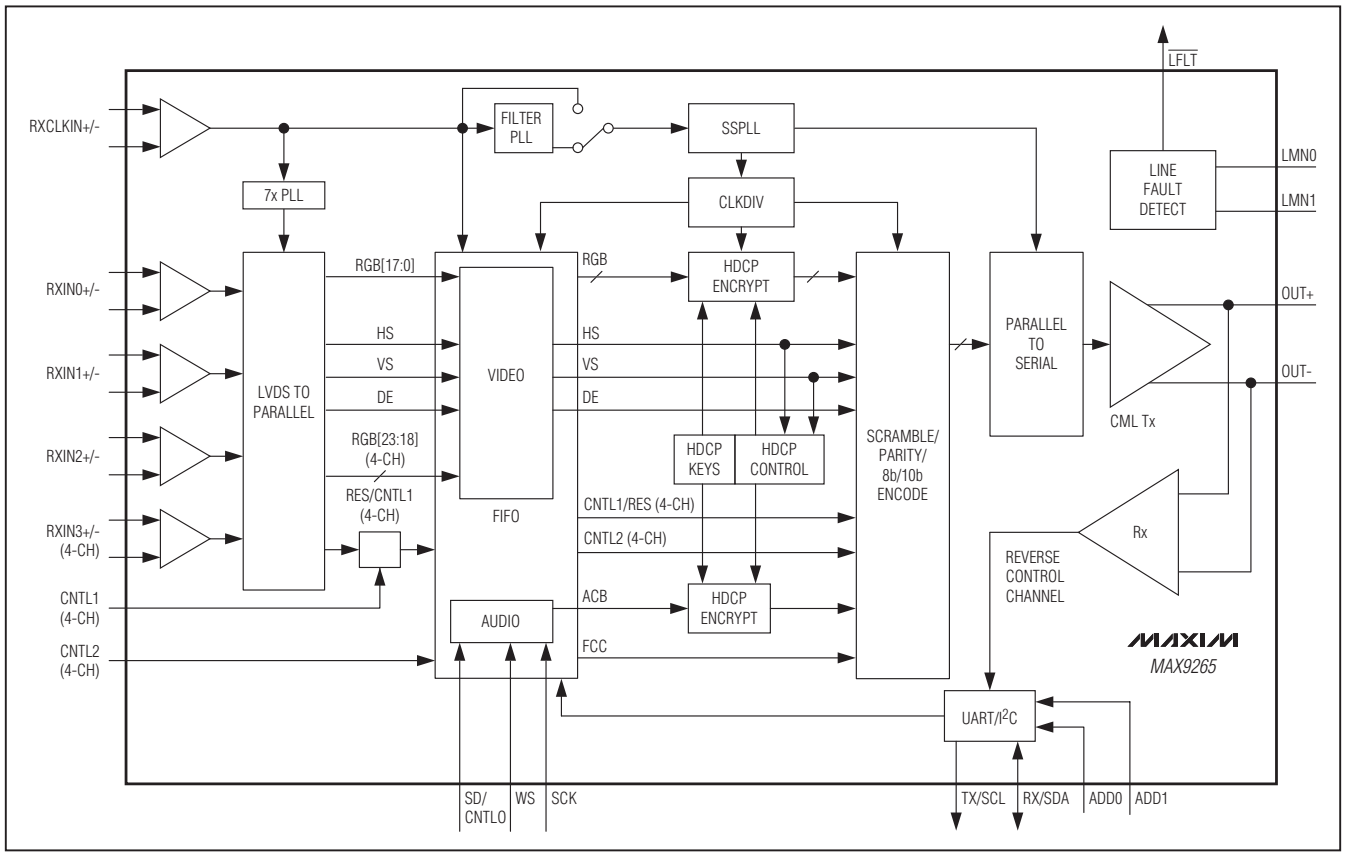
PIN	NAME	FUNCTION
12	RXIN3+	Differential LVDS Data Input 3+. RXIN3+ is not available in 3-channel mode. To use RXIN3+, drive BWS high (4-channel mode) (see Table 3).
15, 32, 47	AVDD	1.8V Analog Power Supply. Bypass AVDD to AGND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to AVDD.
16	SD/CNTL0	I²S Serial-Data Input with Internal Pulldown to GND. Disable I²S to use SD/CNTL0 as an additional control/data input latched every RXCLKIN_ cycle (Figure 7). Encrypted when HDCP is enabled.
17	SCK	I²S Serial-Clock Input with Internal Pulldown to GND
18	WS	I²S Word-Select Input with Internal Pulldown to GND
19	CNTL1	Control Input 1 with Internal Pulldown to GND. Data is latched every RXCLKIN cycle (Figure 7). CNTL1 is not available in 3-channel mode. To use CNTL1, drive BWS high (4-channel mode). CNTL1 or RES (RES from VESA Standard Panel Specification) is mapped to DIN27 (see the *Reserved Bit (RES)* section). CNTL1 is not encrypted when HDCP is enabled (see Table 3).
20	CNTL2	Control Input 2 with Internal Pulldown to GND. Data is latched every RXCLKIN cycle (Figure 7). CNTL2 is not available in 3-channel mode. To use CNTL2, drive BWS high (4-channel mode). CNTL2 is mapped to DIN28. CNTL2 is not encrypted when HDCP is enabled (see Table 3).
22, 39	DVDD	1.8V Digital Power Supply. Bypass DVDD to GND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD.
23, 38	GND	Digital and I/O Ground
24, 37	IOVDD	I/O Supply Voltage. 1.8V to 3.3V logic I/O power supply. Bypass IOVDD to GND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smallest value capacitor closest to IOVDD.
25	RX/SDA	Receive/Serial Data. UART receive or I²C serial-data input/output with internal 30kΩ pullup to IOVDD. In UART mode, RX/SDA is the Rx input of the serializer's UART. In the I²C mode, RX/SDA is the SDA input/output of the MAX9265's I²C master. RX/SDA has an open-drain driver and requires a pullup resistor.
26	TX/SCL	Transmit/Serial Clock. UART transmit or I²C serial-clock output with internal 30kΩ pullup to IOVDD. In UART mode, TX/SCL is the Tx output of the MAX9265's UART. In the I²C mode, TX/SCL is the SCL output of the serializer's I²C master. TX/SCL has an open-drain driver and requires a pullup resistor.
27	SSEN	Spread-Spectrum Enable. Serial link spread-spectrum enable input requires external pulldown or pullup resistor. The state of SSEN latches upon power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). Set SSEN = high for ±0.5% spread spectrum on the serial link. Set SSEN = low to use the serial link without spread spectrum.
28	LMN1	Line-Fault Monitor Input 1 (See Figure 3 for Details)
30, 31	OUT-, OUT+	Differential CML Output -/+. Differential outputs of the serial link.
33	LMN0	Line-Fault Monitor Input 0 (See Figure 3 for Details)
34	$\overline{LFLT}$	Line Fault. Active-low open-drain line-fault output. $\overline{LFLT}$ has a 60kΩ internal pullup resistor. $\overline{LFLT}$ = low indicates a line fault. $\overline{LFLT}$ is high impedance when $\overline{PWDN}$ = low.
35	INT	Interrupt Output. INT indicates remote-side requests. INT = low upon power-up and when $\overline{PWDN}$ = low. A transition on the INT input of the GMSL deserializer toggles the MAX9265's INT output.

HDCP Gigabit Multimedia Serial Link Serializer with LVDS System Interface

Pin Description (continued)

PIN	NAME	FUNCTION
36	DRS	Data-Rate Select. Data-rate range-selection input requires external pulldown or pullup resistor. The state of DRS latches upon power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). Set DRS = high for RXCLKIN frequencies of 8.33MHz to 16.66MHz (3-channel mode) or 6.25MHz to 12.5MHz (4-channel mode). Set DRS = low for RXCLKIN frequencies of 16.66MHz to 104MHz (3-channel mode) or 12.5MHz to 78MHz (4-channel mode).
40	ADD0	Address Selection Input 0. Three-level input to select the MAX9265's device address (see Table 2). The state of ADD0 latches upon power-up or when resuming from power-down mode ($\overline{PWDN}$ = low).
41	BWS	Bus-Width Select Input. BWS requires external pulldown or pullup resistor. Set BWS = low for 3-channel mode. Set BWS = high for 4-channel mode.
42	$\overline{PWDN}$	Active-Low Power-Down Input. $\overline{PWDN}$ requires external pulldown or pullup resistor.
43	CDS	Control Direction Selection. Control link direction selection input requires external pulldown or pullup resistor. Set CDS = low for µC use on the MAX9265 side of the serial link. Set CDS = high for µC use on the GMSL deserializer side of the serial link.
44	MS	Mode Select. Control link mode selection input requires external pulldown or pullup resistor. Set MS = low to select base mode. Set MS = high to select bypass mode.
45	$\overline{AUTOS}$	Active-Low Autostart Setting. $\overline{AUTOS}$ requires external pulldown or pullup resistor. Set $\overline{AUTOS}$ = high to power up the device with no link active. Set $\overline{AUTOS}$ = low to have the serializer power up the serial link with autorange detection (see Tables 9 and 10).
46	ADD1	Address Selection Input 1. Three-level input to select the serializer's device address (see Table 2). The state of ADD1 latches upon power-up or when resuming from power-down mode ($\overline{PWDN}$ = low).
—	EP	Exposed Pad. EP internally is connected to AGND. **MUST** connect EP to the AGND plane for proper thermal and electrical performance.

Functional Diagram



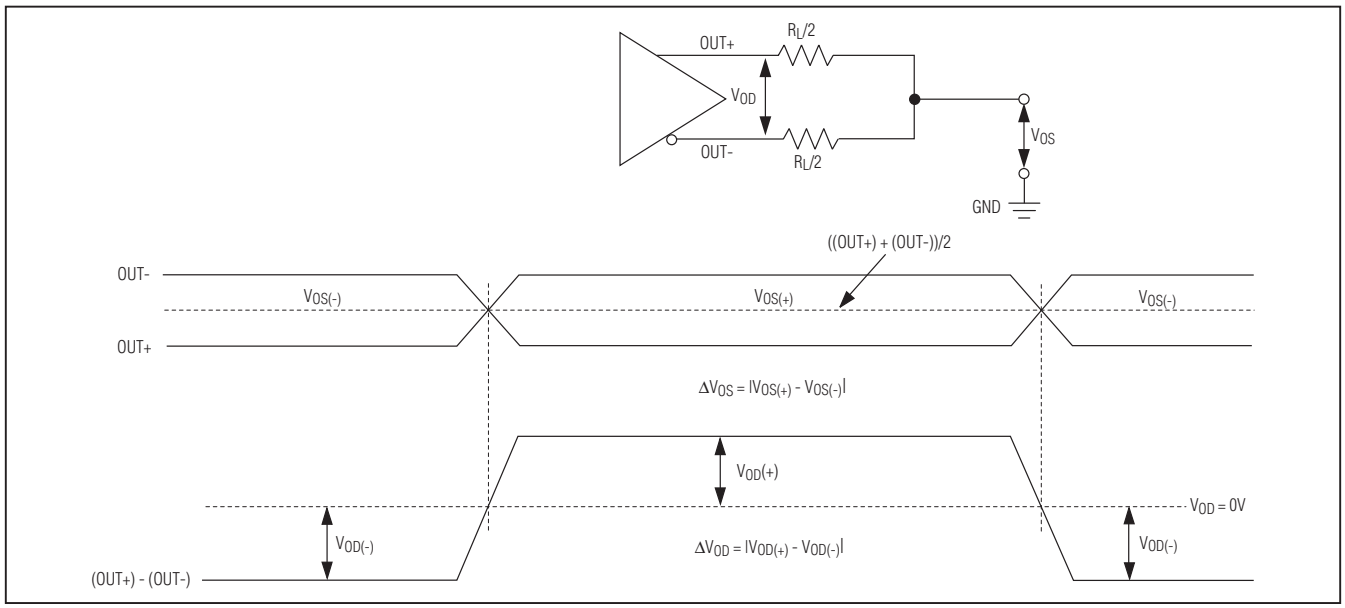


Figure 1. Serial-Output Parameters

HDCP Gigabit Multimedia Serial Link Serializer with LVDS System Interface

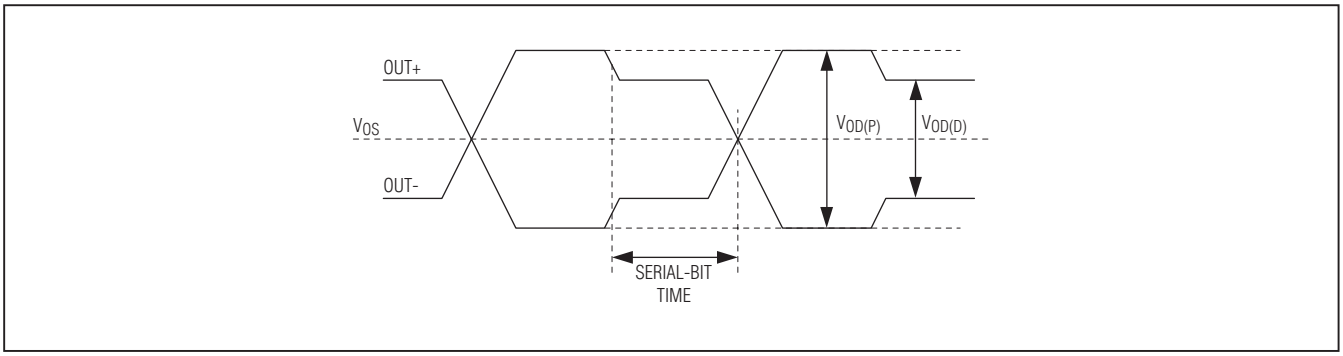


Figure 2. Output Waveforms at OUT+, OUT-

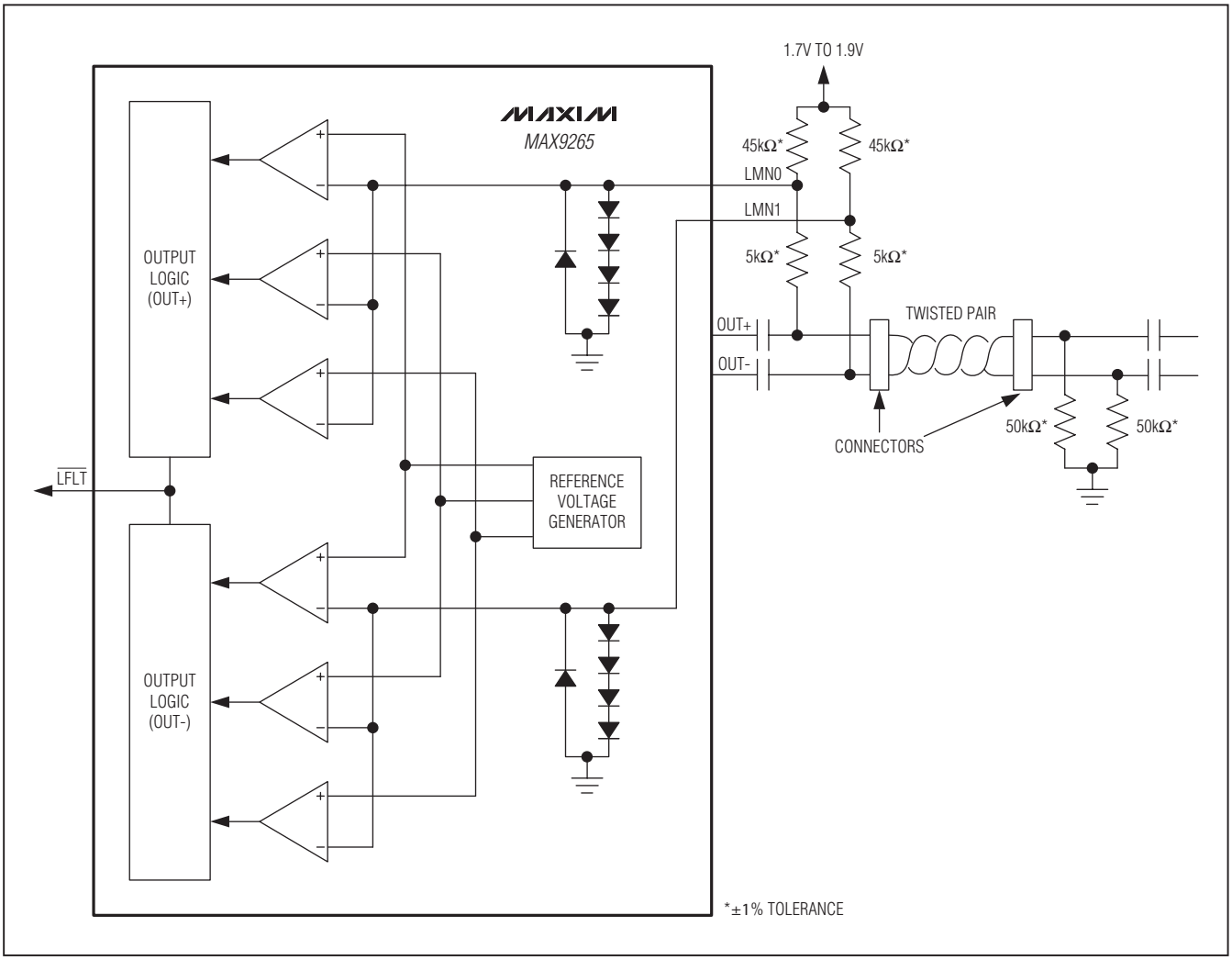


Figure 3. Line-Fault Detector Circuit

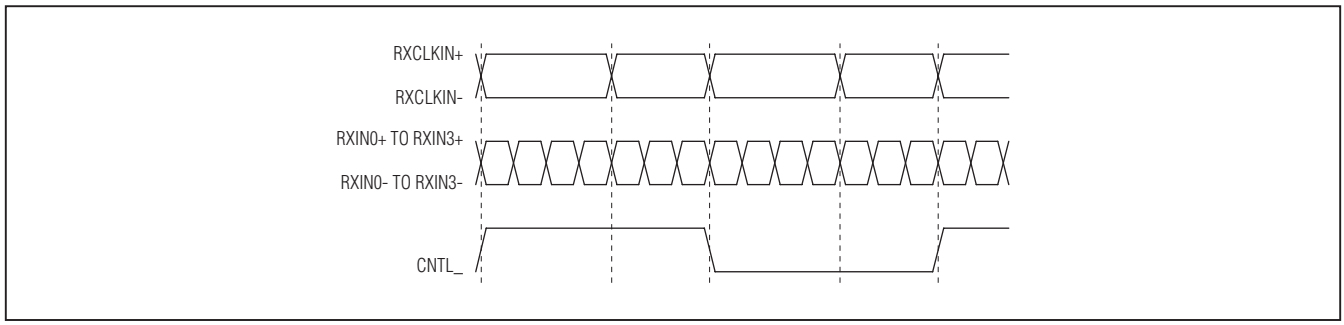


Figure 4. Worst-Case Pattern Input

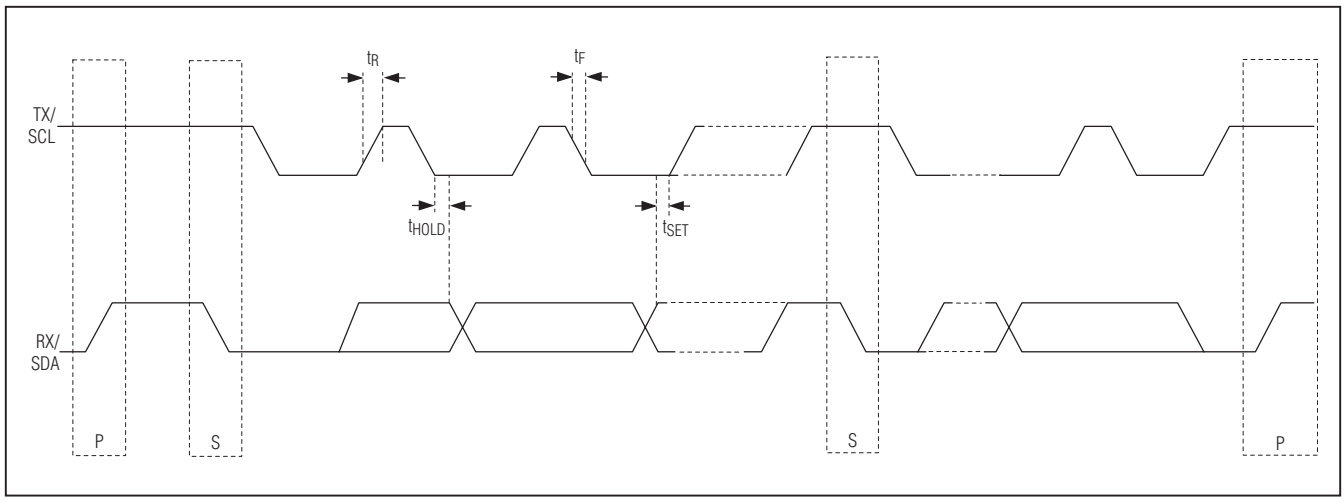


Figure 5. I²C Timing Parameters

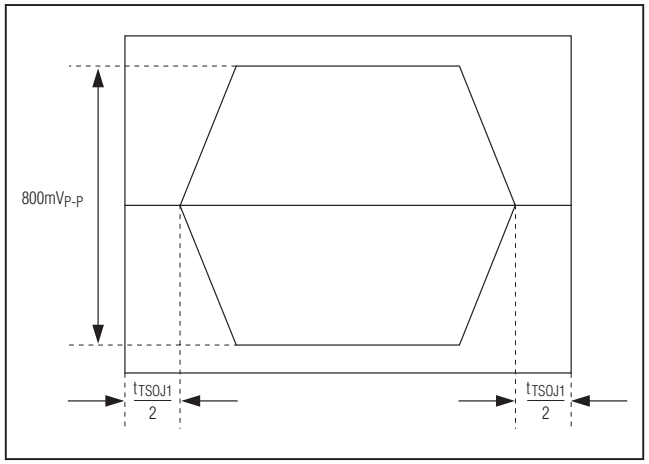


Figure 6. Differential Output Template

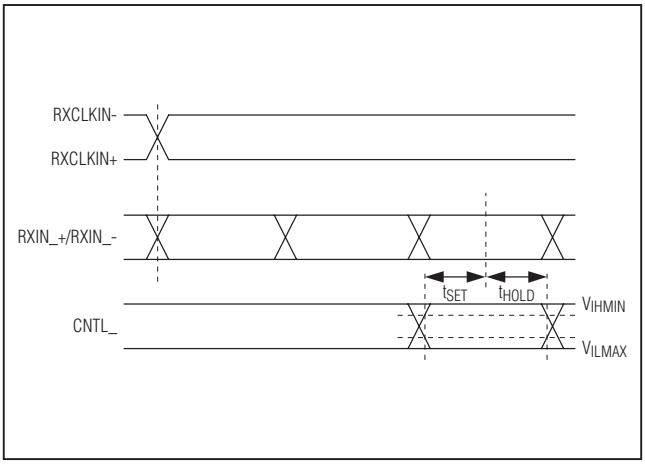


Figure 7. Input Setup and Hold Times

HDCP Gigabit Multimedia Serial Link Serializer with LVDS System Interface

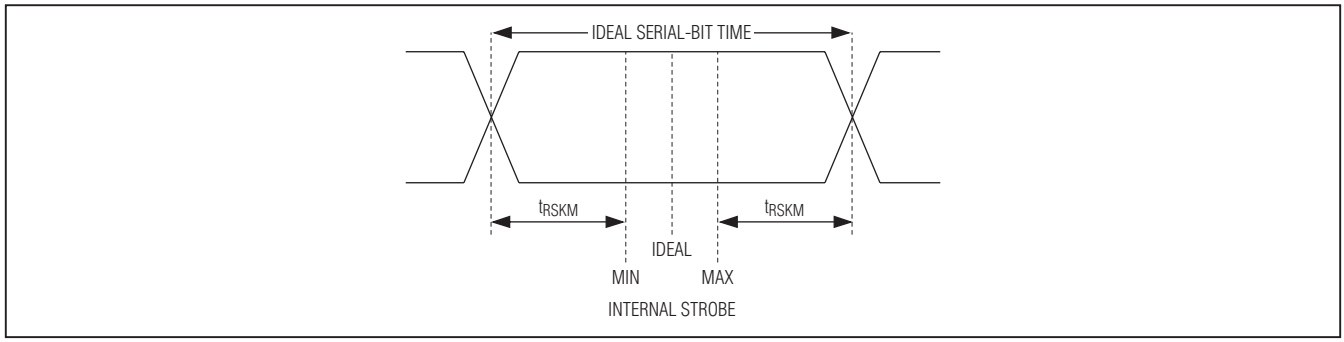


Figure 8. LVDS Receiver Input Skew Margin

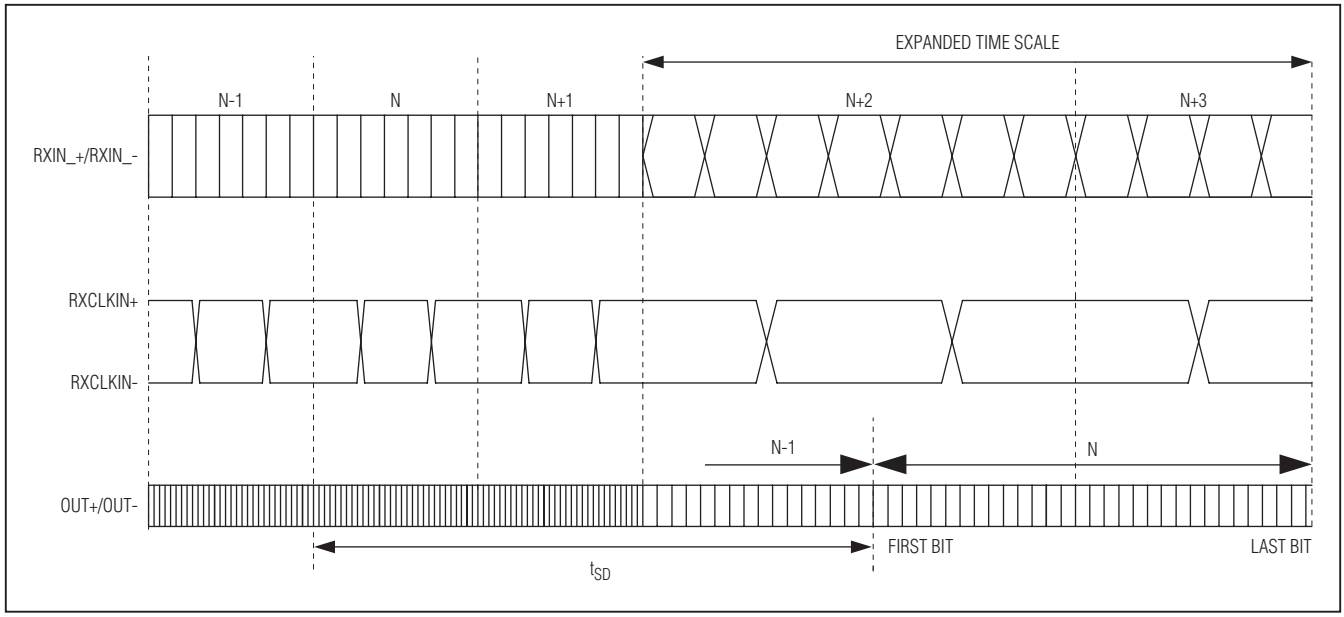


Figure 9. Serializer Delay

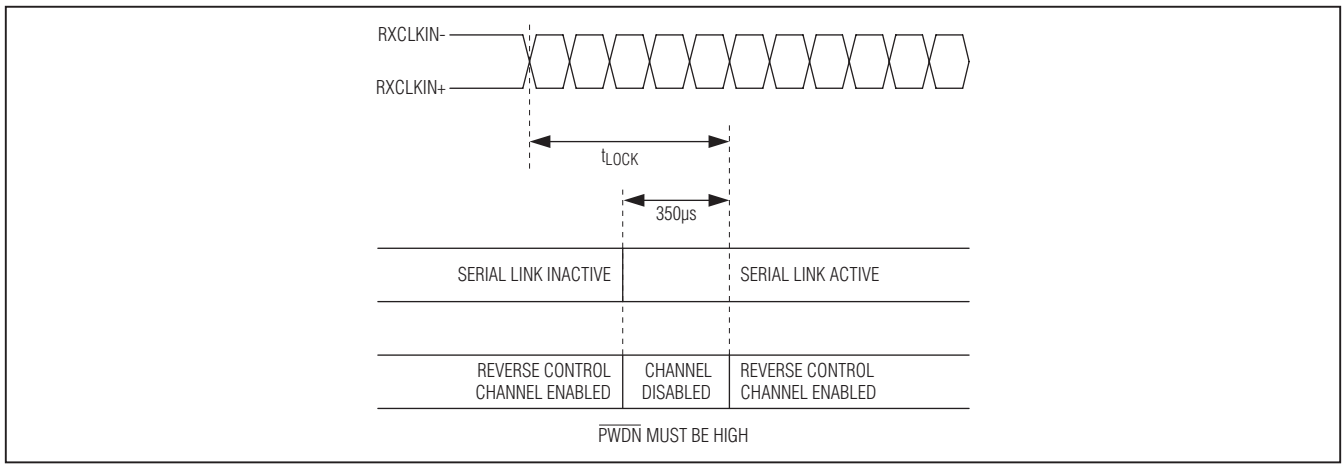


Figure 10. Link Startup Time

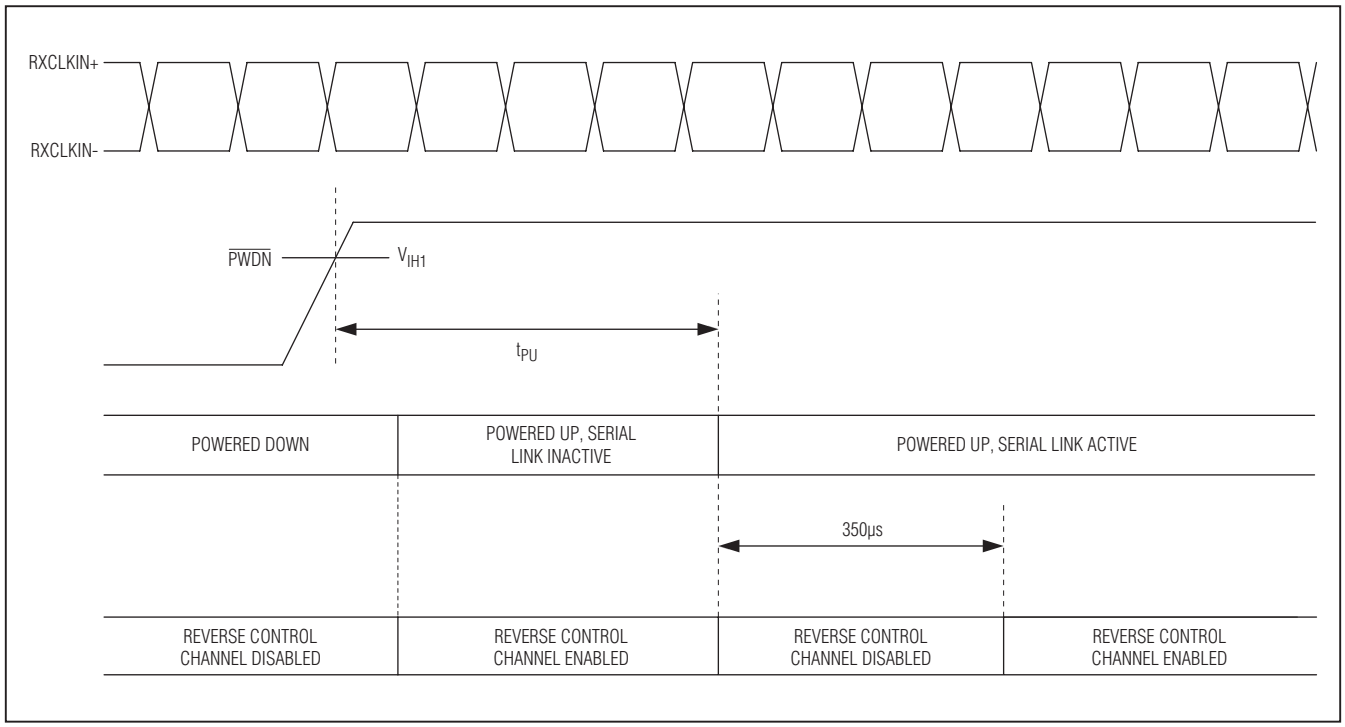


Figure 11. Power-Up Delay

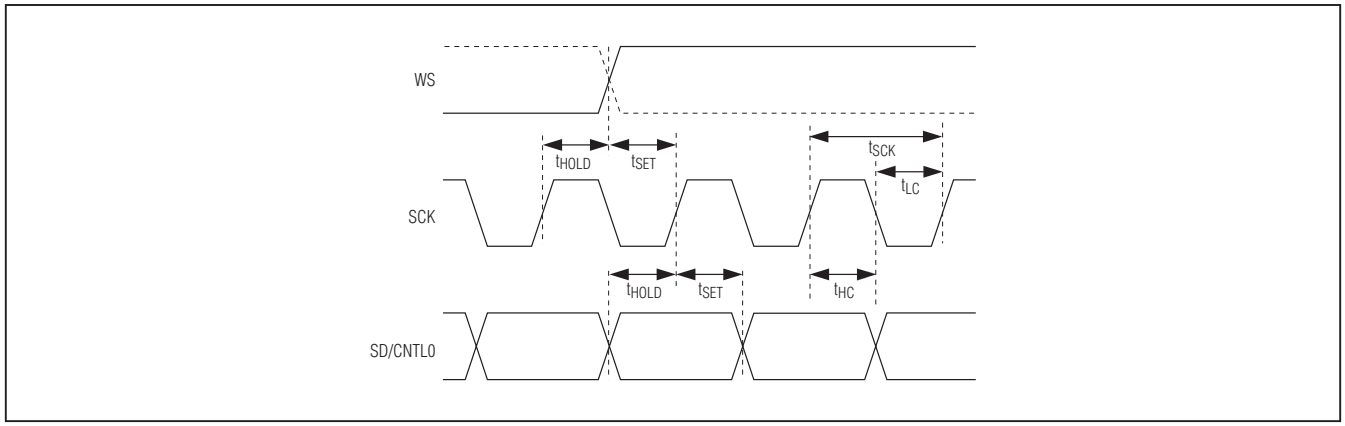


Figure 12. Input I²S Timing Parameters

HDCP Gigabit Multimedia Serial Link Serializer with LVDS System Interface

Detailed Description

The MAX9265 GMSL serializer with LVDS interface utilizes Maxim's GMSL technology and HDCP. When HDCP is enabled, the serializer encrypts video and audio data on the serial link. When HDCP is disabled, the serializer is backward compatible with the MAX9249 LVDS input serializer.

The serializer has a maximum serial payload data rate of 2.5Gbps for 15m or more of shielded twisted-pair (STP) cable. The serializer operates up to a maximum input clock of 104MHz for 3-channel mode, or 78MHz for 4-channel mode, respectively. This serial link supports a wide range of display panels from QVGA (320 x 240) up to WXGA (1280 x 800) and higher with 24-bit color.

The 3-channel mode handles three lanes of LVDS data (21 bits), UART control signals, and three audio signals. The 4-channel mode handles four lanes of LVDS data (28 bits), UART control signals, three audio signals, and auxiliary parallel inputs. The three audio inputs form a standard I²S interface, supporting sample rates from 8kHz to 192kHz and audio word lengths of 4 to 32 bits. The embedded control channel forms a full-duplex, differential 9.6kbps to 1Mbps UART link between the serializer and deserializer for HDCP-related control operations. In addition, the control channel enables electronic control unit (ECU) or microcontroller (µC) control of peripherals in the remote side, such as backlight control, gray-scale Gamma correction, camera module, and touch screen. An ECU/µC can be located on the serializer side of the link (typical for video display), on the GMSL deserializer side of the link (typical for image sensing), or on both sides. Base-mode communication with peripherals uses either I²C or the GMSL UART format. A bypass mode enables full-duplex communication using a user-defined UART format.

The serializer pre/deemphasis, along with the GMSL deserializer channel equalizer, extends the link length and enhances the link reliability. Spread spectrum is available to reduce EMI on the serial output. The CML and LVDS connections comply with ISO 10605 and IEC 61000-4-2 ESD protection standards.

Register Mapping

The µC configures various operating conditions of the serializer and the GMSL deserializer through internal registers. Table 1 lists the default register values for the serializer. The device addresses are stored in registers 0x00 and 0x01 of both the serializer and the GMSL deserializer. Write to registers 0x00 and 0x01 in both devices to change the device address of the serializer or the GMSL deserializer.

HDCP Bitmapping and Bus-Width Selection

The LVDS input has two selectable modes, 3-channel mode and 4-channel mode. In 3-channel mode, RXIN3_ is not used. For both modes, the SD/CNTL0, SCK, and WS pins are for I²S audio. The serializer uses RXCLKIN rates from 8.33MHz to 104MHz for 3-channel mode and 6.25MHz to 78MHz for 4-channel mode.

Table 3 lists the bit mapping for the LVDS input. The serializer has HDCP encryption on 18 RGB input bits and the I²S input. Four-channel mode has additional HDCP encryption on the additional RGB bits.

The control signals (CNTL_) do not have HDCP encryption. SD/CNTL0, when used as an additional control input (AUDIOEN = 0), also does not have HDCP encryption.

Table 1. Power-Up Default Register Map (see Table 17 and Table 18)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x00	0x40, 0x48, 0x48, 0x80, 0x84, 0x88, 0xC0, 0xC4, 0xC8	SERID = XX00XX0, serializer device address is determined by ADD0 and ADD1 (Table 2) CFGBLOCK = 0, registers 0x00 to 0x1F are read/write
0x01	0x50, 0x58, 0x58, 0x90, 0x94, 0x98, 0xD0, 0xD4, 0xD8	DESID = XX00XX0, deserializer device address is determined by ADD0 and ADD1 (Table 2) RESERVED = 0
0x02	0x1F, 0x3F	SS = 000 (SSEN = low), SS = 001 (SSEN = high), spread-spectrum settings depend on SSEN pin state at power-up AUDIOEN = 1, I²S channel enabled PRNG = 11, automatically detect the pixel clock range SRNG = 11, automatically detect serial-data rate
0x03	0x00	AUTOFM = 00, calibrate spread-modulation rate only once after locking SDIV = 000000, autocalibrate the sawtooth divider
0x04	0x03, 0x13, 0x83, or 0x93	SEREN = 0 ($\overline{AUTOS}$ = high), SEREN = 1 ($\overline{AUTOS}$ = low), serial link enable default depends on $\overline{AUTOS}$ pin state at power-up CLINKEN = 0, configuration link disabled PRBSEN = 0, PRBS test disabled SLEEP = 0 or 1, sleep mode state depends on CDS and $\overline{AUTOS}$ pin state at power-up (see the *Link Startup Procedure* section) INTTYPE = 00, base mode uses I²C REVCCEN = 1, reverse control channel active (receiving) FWDCCEN = 1, forward control channel active (sending)
0x05	0x70	I2CMETHOD = 0, I²C packets include register address DISFPLL = 1, filter PLL disabled CMLLVL = 11, 400mV CML signal level PREEMP = 0000, preemphasis disabled
0x06	0x40	RESERVED = 01000000
0x07	0x22	RESERVED = 00100010
0x08	0x0A (read only)	RESERVED = 0000 LFNEG = 10, no faults detected LFPOS = 10, no faults detected
0x0C	0x70	RESERVED = 01110000
0x0D	0x0F	SETINT = 0, interrupt output set to low INVVSYNC = 0, serializer does not invert VSYNC INVHSYNC = 0, serializer does not invert HSYNC DISRES = 0, RES mapped to DIN27 SKEWADJ = 1111, No X7PLL clock skew adjust
0x1E	0x07 (read only)	ID = 00000111, device ID is 0x07

HDCP Gigabit Multimedia Serial Link Serializer with LVDS System Interface

Table 1. Power-Up Default Register Map (see Table 17 and Table 18) (continued)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x1F	0x1X (read only)	RESERVED = 000 CAPS = 1, serializer is HDCP capable REVISION = XXXX, revision number
0x80 to 0x84	0x0000000000	BKSV = 0x0000000000, HDCP receiver KSV is 0x0000000000
0x85 to 0x86	0x0000	RI = 0x0000, RI of the transmitter is 0x0000
0x87	0x00	PJ = 0x00, PJ of the transmitter is 0x00
0x88 to 0x8F	0x0000000000000000 (read only)	AN = 0000000000000000, session random number (read only)
0x90 to 0x94	0xXXXXXXXXXX (read only)	AKSV = 0xXXXXXXXXXXXXXXXX, HDCP transmitter KSV is 0xXXXXXXXXXX (read only)
0x95	0x00	PD_HDCP = 0, HDCP circuits powered up EN_INT_COMP = 0, internal link verification disabled FORCE_AUDIO = 0, normal I²S audio operation FORCE_VIDEO = 0, normal video link operation RESET_HDCP = 0, normal HDCP operation START_AUTHENTICATION = 0, HDCP authentication not started VSYNC_DET = 0, VSYNC rising edge not detected ENCRYPTION_ENABLE = 0, HDCP encryption disabled
0x96	0x00 (read only)	RESERVED = 0000 V_MATCHED = 0, SHA-1 hash value not matched PJ_MATCHED = 0, enhanced link verification response not matched R0_RI_MATCHED = 0, link verification response not matched BKSV_INVALID = 0, invalid receiver KSV
0x97	0x00	RESERVED = 0000000 REPEATER = 0, HDCP receiver is not a repeater
0x98 to 0x9C	0x0000000000	ASEED = 0x0000000000, optional RNG seed value is 0x0000000000
0x9D to 0x9F	0x000000	DFORCE = 0x000000, video data forced to 0x000000 when FORCE_VIDEO = 1
0xA0 to 0xA3	0x00000000	H0 part of SHA-1 hash value is 0x00000000
0xA4 to 0xA7	0x00000000	H1 part of SHA-1 hash value is 0x00000000
0xA8 to 0xAB	0x00000000	H2 part of SHA-1 hash value is 0x00000000
0xAC to 0xAF	0x00000000	H3 part of SHA-1 hash value is 0x00000000
0xB0 to 0xB3	0x00000000	H4 part of SHA-1 hash value is 0x00000000
0xB4	0x00	Reserved = 0000 MAX_CASCADE_EXCEEDED = 0, less than 7 cascaded HDCP devices attached DEPTH = 000, device cascade depth is zero
0xB5	0x00	MAX_DEVS_EXCEEDED = 0, less than 127 HDCP devices attached DEVICE_COUNT = 0000000, zero attached devices
0xB6	0x00	GPMEM = 00000000, 0x00 stored in general-purpose memory
0xB7 to 0xB9	0x000000	Reserved = 0x000000
0xBA to 0xFF	All zero	KSV_LIST = all zero, no KSVs stored

X = Don't care.

Table 2. Device Address Defaults (Register 0x00, 0x01)

PIN		DEVICE ADDRESS (bin)								SERIALIZER DEVICE ADDRESS (hex)	DESERIALIZER DEVICE ADDRESS (hex)
ADD1	ADD0	D7	D6	D5	D4	D3	D2	D1	D0		
Low	Low	1	0	0	X*	0	0	0	R/$\overline{W}$	80	90
Low	High	1	0	0	X*	0	1	0	R/$\overline{W}$	84	94
Low	Open	1	0	0	X*	1	0	0	R/$\overline{W}$	88	98
High	Low	1	1	0	X*	0	0	0	R/$\overline{W}$	C0	D0
High	High	1	1	0	X*	0	1	0	R/$\overline{W}$	C4	D4
High	Open	1	1	0	X*	1	0	0	R/$\overline{W}$	C8	D8
Open	Low	0	1	0	X*	0	0	0	R/$\overline{W}$	40	50
Open	High	0	1	0	X*	0	1	0	R/$\overline{W}$	44	54
Open	Open	0	1	0	X*	1	0	0	R/$\overline{W}$	48	58

**X = 0 for the serializer address, X = 1 for the deserializer address.*

Table 3. LVDS, HDCP Mapping and Bus Width Selection (see Figures 13 and 14)

INPUT BITS	3-CHANNEL MODE (BWS = LOW)			4-CHANNEL MODE (BWS = HIGH)		
	BITMAPPING	AUXILIARY SIGNALS MAPPING	HDCP ENCRYPTION CAPABILITY	BITMAPPING	AUXILIARY SIGNALS MAPPING	HDCP ENCRYPTION CAPABILITY
DIN[0:5]	R[0:5]	—	Yes	R[0:5]	—	Yes
DIN[6:11]	G[0:5]	—	Yes	G[0:5]	—	Yes
DIN[12:17]	B[0:5]	—	Yes	B[0:5]	—	Yes
DIN[18:20]	HS, VS, DE	—	No	HS, VS, DE	—	No
DIN[21:22]	Not available	—	—	R6, R7	—	Yes
DIN[23:24]	Not available	—	—	G6, G7	—	Yes
DIN[25:26]	Not available	—	—	B6, B7	—	Yes
DIN27	Not available	Not available	—	RES*	CNTL1*	No
DIN28	—	Not available	—	—	CNTL2	No
SD	—	SD/CNTL0	I^2S**	—	SD/CNTL0	I^2S**

**See the* Reserved Bit (RES) *section for details.*
***HDCP encryption on SD when used as an I^2S signal.*

HDCP Gigabit Multimedia Serial Link Serializer with LVDS System Interface

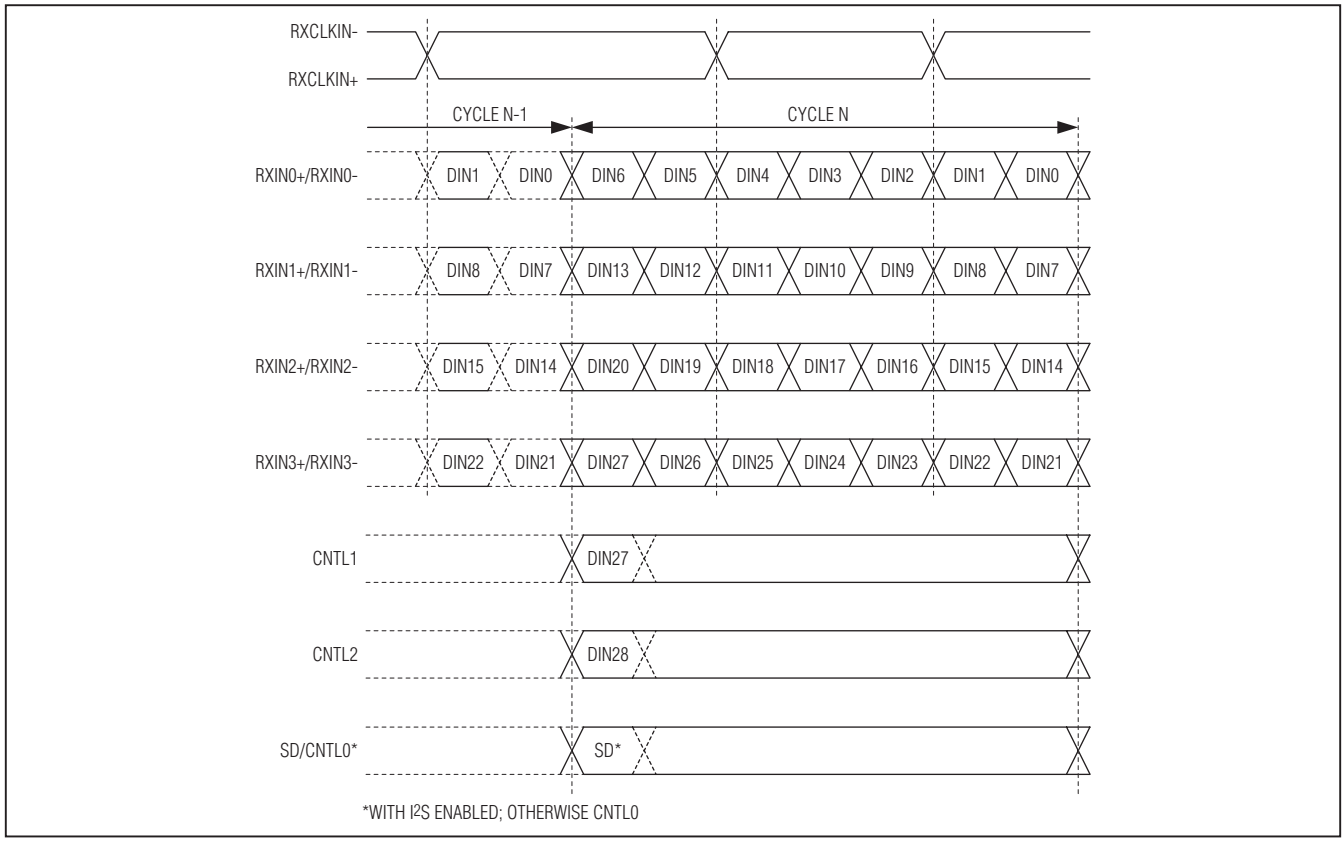


Figure 13. LVDS Input Timing

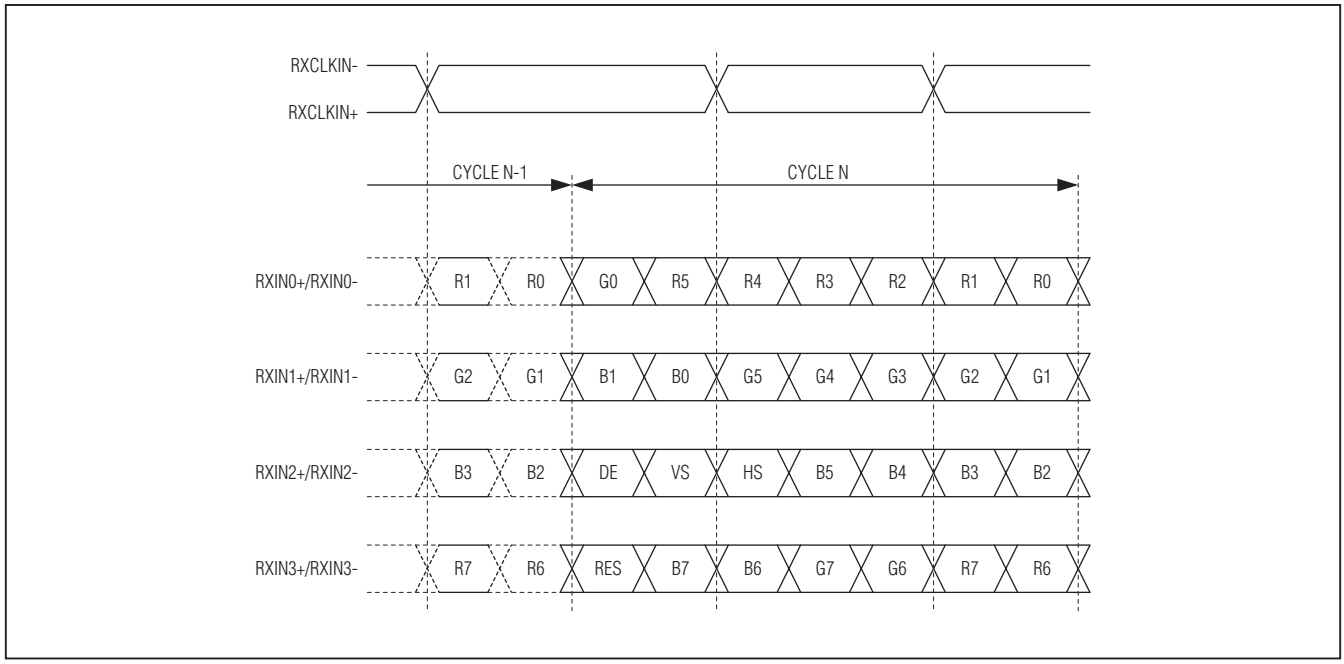


Figure 14. Panel Clock and Bit Assignment

Serial Link Signaling and Data Format

The serializer uses CML signaling with programmable pre-emphasis and AC-coupling. The GMSL deserializer uses AC-coupling and programmable channel equalization. Together, the GMSL link can operate at full speed over STP cable lengths to 15m or more.

In addition to HDCP encryption (when enabled), the serializer scrambles and encodes the input data and sends the 8b/10b coded signal through the serial link. Figures 15 and 16 show the serial-data packet format before HDCP encryption, scrambling and 8b/10b encoding. In 3-channel or 4-channel mode, 21 or 29 bits map from the LVDS input. The audio channel bit (ACB) contains an encoded audio signal derived from the three I²S signals (SD, SCK, and WS). The forward control-channel (FCC) bit carries the forward control data. The last bit (PCB) is the parity bit of the previous 23 or 31 bits.

Reserved Bit (RES)

In 4-channel mode, the serializer serializes all bits of all four lanes, including RES, by default. Set DISRES (D4 of register 0x0D) to 1 to map CNTL1 to DIN27 instead of RES.

Reverse Control Channel

The serializer uses the reverse control channel to receive I²C/UART and interrupt signals from the GMSL deserializer in the opposite direction of the video stream. The reverse control channel and forward video data coexist on the same twisted pair forming a bidirectional link. The reverse control channel operates independently from the forward control channel. The reverse control channel is available 500µs after power-up. The serializer temporarily disables the reverse control channel for 350µs after starting/stopping the forward serial link.

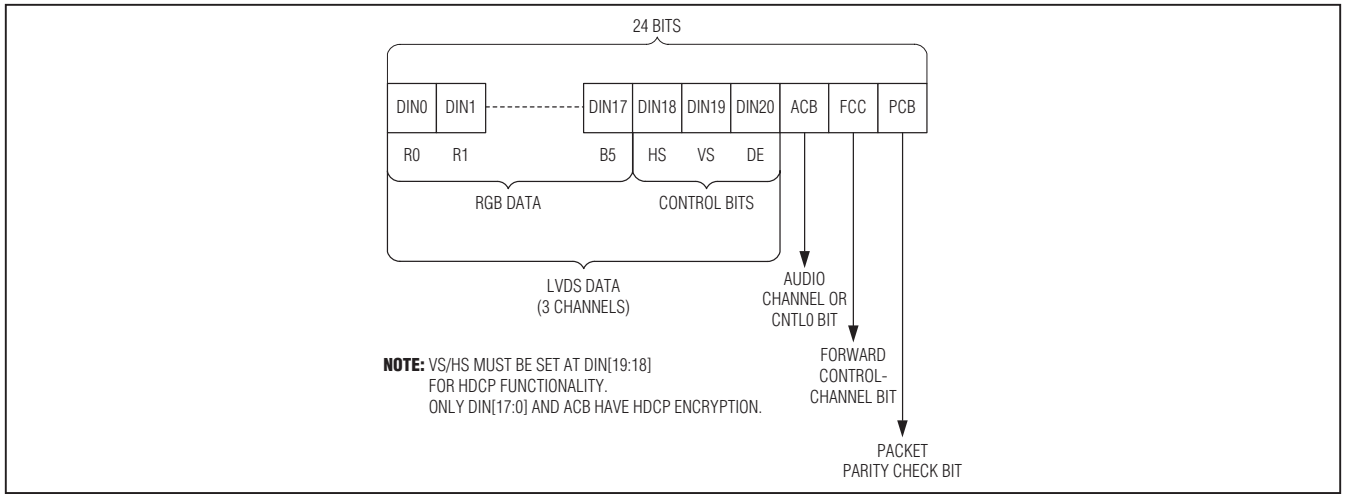


Figure 15. 3-Channel Mode Serial Link Data Format

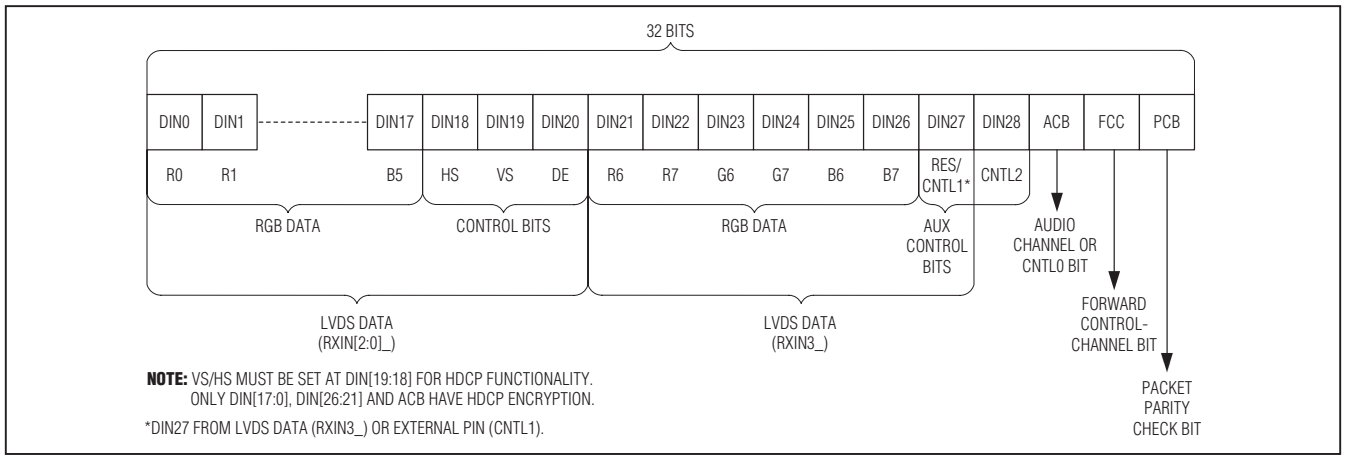


Figure 16. 4-Channel Mode Serial Link Data Format

HDCP Gigabit Multimedia Serial Link Serializer with LVDS System Interface

Data-Rate Selection

The serializer uses the DRS input to set the RXCLKIN_ frequency range. Set DRS high for an RXCLKIN_ frequency range of 6.25MHz to 12.5MHz (4-channel mode) or 8.33MHz to 16.66MHz (3-channel mode). Set DRS low for normal operation with an RXCLKIN_ frequency range of 12.5MHz to 78MHz (4-channel mode) or 16.66MHz to 104MHz (3-channel mode).

Audio Channel

The I²S audio channel supports audio sampling rates from 8kHz to 192kHz, and audio word lengths from 4 bits to 32 bits. The audio bit clock (SCK) does not have to be synchronized with RXCLKIN_. The serializer automatically encodes audio data into a single bit stream synchronous with RXCLKIN_. The GMSL deserializer decodes the audio stream and stores audio words in a FIFO. Audio rate detection uses an internal oscillator to continuously determine the audio data rate and output the audio in I²S format. The audio channel is enabled by default. When the audio channel is disabled, SD/CNTL0 on the serializer and GMSL deserializer is treated as an additional control signal (CNTL0).

Since the audio data sent through the serial link is synchronized with RXCLKIN, low RXCLKIN_ frequencies limit the maximum audio sampling rate. Table 4 lists the maximum audio sampling rate for various RXCLKIN_ frequencies. Spread-spectrum settings do not affect the I²S data rate or WS clock frequency.

Control Channel and Register Programming

The control channel is available for the µC to send and receive control data over the serial link simultaneously with the high-speed data. Configuring the CDS pin allows the µC to control the link from either the serializer or the GMSL deserializer side to support video-display or image-sensing applications. The control channel between the µC and serializer or GMSL deserializer runs in base mode or bypass mode according to the mode selection (MS) input of the device connected to the µC. Base mode is a half-duplex control channel and the bypass mode is a full-duplex control channel.

Base Mode

In base mode, the µC is the host and can access the core and HDCP registers of both the serializer and GMSL deserializer from either side of the link by using the GMSL UART protocol. The µC can also program the peripherals on the remote side by sending the UART packets to the serializer or GMSL deserializer, with the UART packets converted to I²C by the device on the remote side of the link (GMSL deserializer for LCD or serializer for image-sensing applications). The µC communicates with a UART peripheral in base mode (through INTTYPE register settings), using the half-duplex default GMSL UART protocol of the serializer/GMSL deserializer. The device addresses of the serializer and GMSL deserializer in base mode are programmable. The default value is determined by the pin settings of ADD0 and ADD1 (Table 2).

When the peripheral interface uses I²C (default), the serializer/GMSL deserializer convert packets to I²C that have device addresses different from those of the serializer or GMSL deserializer. The converted I²C bit rate is the same as the original UART bit rate.

The GMSL deserializer uses a proprietary differential line coding to send signals back towards the serializer. The speed of the control channel ranges from 9.6kbps to 1Mbps in both directions. The serializer and GMSL deserializer automatically detect the control-channel bit rate in base mode. Packet bit rates can vary up to 3.5x from the previous bit rate (see the *Changing the Clock Frequency* section).

Figure 17 shows the UART protocol for writing and reading in base mode between the µC and the serializer/GMSL deserializer.

Figure 18 shows the UART data format. Figure 19 and Figure 20 detail the formats of the SYNC byte (0x79) and the ACK byte (0xC3). The µC and the connected slave chip generate the SYNC byte and ACK byte, respectively. Events such as device wake-up and interrupt generate transitions on the control channel that should be ignored by the µC. Data written to the serializer/GMSL deserializer registers do not take effect until after the acknowledge byte is sent. This allows the µC to verify write commands received without error, even if the result of the write command directly affects the serial link. The slave uses the SYNC byte to synchronize with the host UART data rate automatically. If the INT or MS inputs of the GMSL deserializer toggles while there is control-channel communication, the control-channel communication can be corrupted. In the event of a missed acknowledge, the µC should assume there was an error in the packet when the slave device receives it, or that an error occurred during the response from the slave device. In base mode, the µC must keep the UART Tx/Rx lines high for 16 bit-times before starting to send a new packet.

Table 4. LVDS, HDCP Mapping and Bus Width Selection (see Figures 13 and 14)

WORD LENGTH (bits)	RXCLKIN_ FREQUENCY (DRS = LOW) (MHz)				RXCLKIN_ FREQUENCY (DRS = HIGH) (MHz)			
	12.5	15	16.6	> 20	6.25	7.5	8.33	> 10
8	> 192	> 192	> 192	> 192	> 192	> 192	> 192	> 192
16	> 192	> 192	> 192	> 192	> 192	> 192	> 192	> 192
18	185.5	> 192	> 192	> 192	185.5	> 192	> 192	> 192
20	174.6	> 192	> 192	> 192	174.6	> 192	> 192	> 192
24	152.2	182.7	> 192	> 192	152.2	182.7	> 192	> 192
32	123.7	148.4	164.3	> 192	123.7	148.4	164.3	> 192

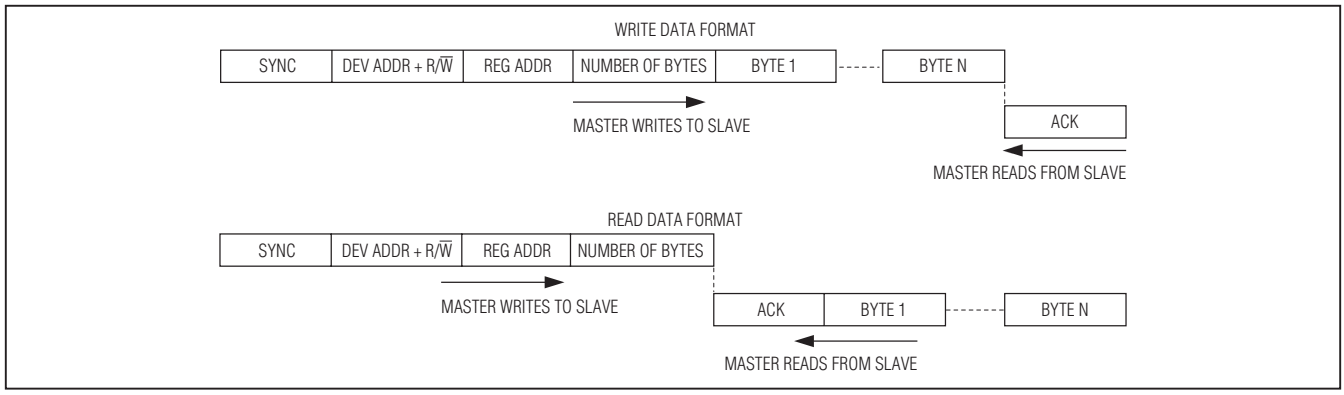


Figure 17. GMSL UART Protocol for Base Mode

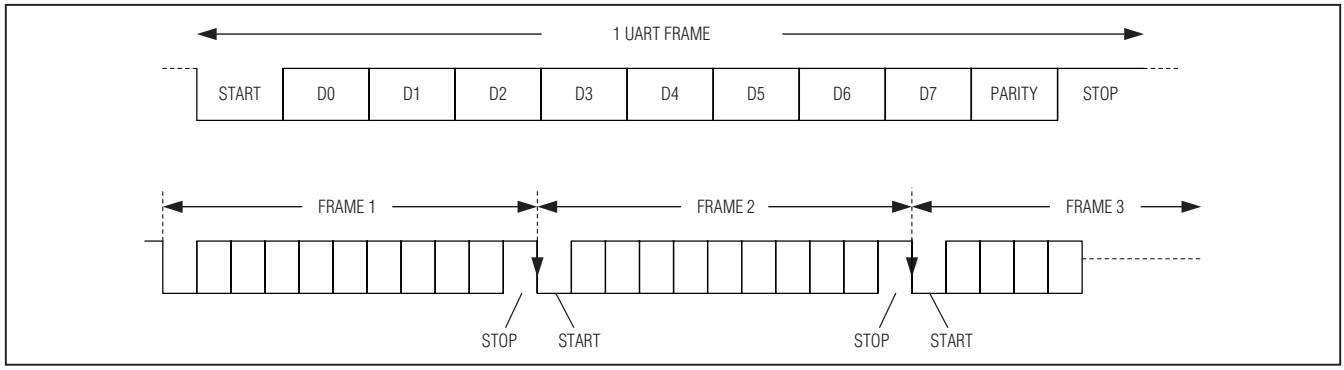


Figure 18. GMSL UART Data Format for Base Mode

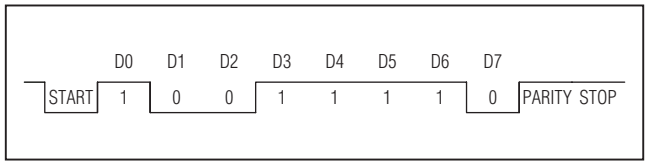


Figure 19. Sync Byte (0x79)

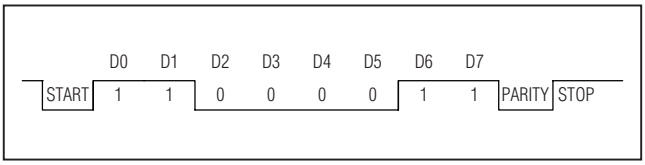


Figure 20. ACK Byte (0xC3)

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As shown in Figure 21, the remote-side device converts the packets going to or coming from the peripherals from the UART format to the I²C format and vice versa. The remote device removes the byte number count and adds or receives the ACK between the data bytes of I²C. The I²C's data rate is the same as the UART data rate.

Interfacing Command-Byte-Only I²C Devices

The serializer and GMSL deserializer UART-to-I²C conversion interfaces with devices that do not require register addresses, such as the MAX7324 GPIO expander. In this mode, the I²C master ignores the register address byte and directly reads/writes the subsequent data bytes (Figure 22). Change the communication method of the I²C master using the I2CMETHOD bit. I2CMETHOD = 1 sets command-byte-only mode, while I2CMETHOD = 0 sets normal mode where the first byte in the data stream is the register address.

Bypass Mode

In bypass mode, the serializer/GMSL deserializer ignore UART commands from the µC and the µC communicates with the peripherals directly using its own defined UART protocol. The µC cannot access the serializer/GMSL deserializer's registers in this mode. Peripherals accessed through the forward control channel using the UART interface need to handle at least one RXCLKIN_ period ±10ns of jitter due to the asynchronous sampling of the UART signal by RXCLKIN_. Set MS = high to put the control channel into bypass mode. For applications with the µC connected to the deserializer (CDS is high), there is a 1ms wait time between setting MS high and the bypass control channel being active. There is no delay time in switching to bypass mode when the µC is connected to the serializer (CDS = low). Bypass mode accepts bit rates down to 9.6kbps in either direction. See the *Interrupt Control* section for interrupt functionality limitations. The control-channel data pattern should not be held low longer than 100µs in either base or bypass mode to ensure proper interrupt functionality.

Interrupt Control

The INT pin of the serializer is the interrupt output and the INT pin of the GMSL deserializer is the interrupt input. The interrupt output on the serializer follows the transitions at the interrupt input. This interrupt function supports remote-side functions such as touch-screen peripherals, remote power-up, or remote monitoring. Interrupts that occur during periods where the reverse control channel is disabled, such as link startup/shutdown, are automatically resent once the reverse control channel becomes available again. Bit D4 of register 0x06 in the GMSL deserializer also stores the interrupt input state. The INT output of the serializer is low after power-up. In addition, the µC can set the INT output of the serializer by writing to the SETINT register bit. In normal operation, the state of the interrupt output changes when the interrupt input on the GMSL deserializer toggles. Do not send a logic-low value longer than 100µs in either base or bypass mode to ensure proper interrupt functionality.

Pre/Deemphasis Driver

The serial line driver in the serializer employs current-mode logic (CML) signaling. The driver can generate an adjustable preemphasized waveform according to the cable length and characteristics. There are 13 preemphasis settings as shown in Table 5. Negative preemphasis levels are deemphasis levels in which the preemphasized swing level is the same as normal swing, but the no-transition data is deemphasized. Program the preemphasis levels through register 0x05 D[3:0] of the serializer. This preemphasis function compensates the high frequency loss of the cable and enables reliable transmission over longer link distances. Additionally, a lower power drive mode can be entered by programming CMLLVL bits (0x05 D[5:4]) to reduce the driver strength down to 75% (CMLLVL = 10) or 50% (CMLLVL = 01) from 100% (CMLLVL = 11, default).

Spread Spectrum

To reduce the EMI generated by the transitions on the serial link, the serializer supports spread spectrum. Turning on spread spectrum on the serializer spreads the serial link, which is tracked by the serializer deserializer. The six selectable spread-spectrum rates at the serial output are ±0.5%, ±1%, ±1.5%, ±2%, ±3%, and ±4% (Table 6). Some spread-spectrum rates can only be used at lower RXCLKIN_ frequencies (Table 7). There is no RXCLKIN_ frequency limit for the 0.5% spread rate.

Set the serializer's SSEN input high to select 0.5% spread at power-up and SSEN input low to select no spread at power-up. The state of SSEN is latched upon power-up or when resuming from power-down mode.

Whenever the serializer's spread spectrum is turned on or off, the serial link automatically restarts and remains unavailable while the GMSL deserializer relocks to the serial data. Turning on spread spectrum on the serializer or GMSL deserializer does not affect the audio data stream.

The serializer includes a sawtooth divider to control the spread-modulation rate. Autodetection or manual programming of the RXCLKIN_ operation range guarantees a spread-spectrum modulation frequency within 20kHz to 40kHz. Additionally, manual configuration of the sawtooth divider (SDIV, 0x03 D[5:0]) allows the user to set a modulation frequency according to the RXCLKIN_ frequency. Always keep the modulation frequency between 20kHz to 40kHz to ensure proper operation.

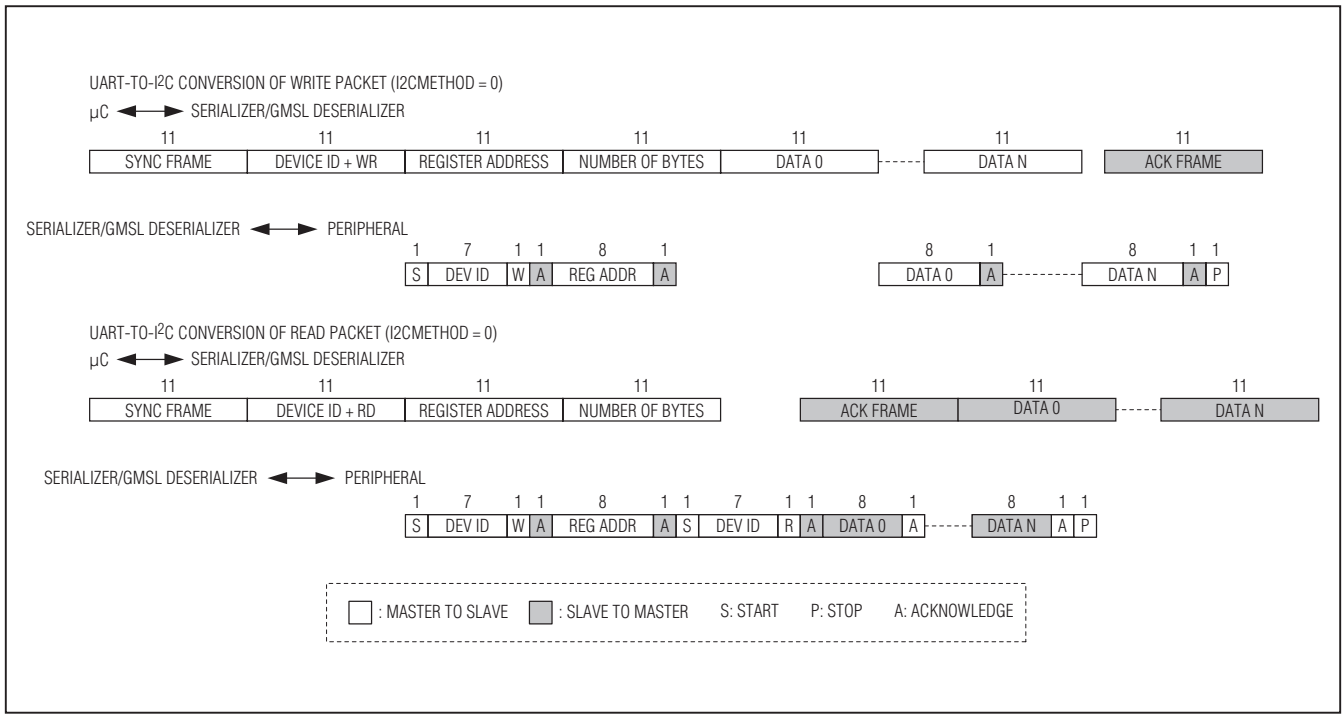

Figure 21. Format Conversion Between GMSL UART and I2C with Register Address (I2CMETHOD = 0)

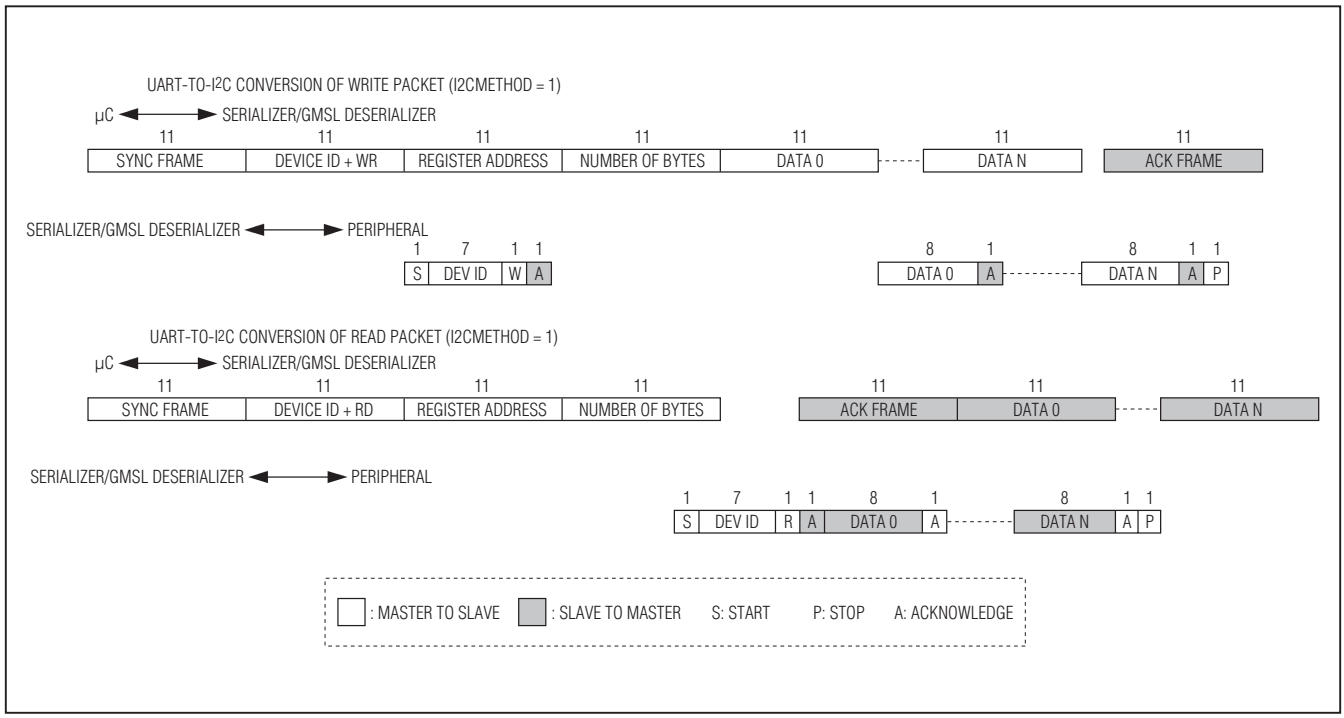

Figure 22. Format Conversion Between GMSL UART and I2C with Register Address (I2CMETHOD = 1)

Table 5. CML Driver Strength (Default Level, CMLLVL = 11)

PREEMPHASIS LEVEL (dB)*	PREEMPHASIS SETTING (0x05, D[3:0])	I_{CML} (mA)	I_{PRE} (mA)	SINGLE-ENDED VOLTAGE SWING	
				MAX (mV)	MIN (mV)
-6.0	0100	12	4	400	200
-4.1	0011	13	3	400	250
-2.5	0010	14	2	400	300
-1.2	0001	15	1	400	350
0	0000	16	0	400	400
1.1	1000	16	1	425	375
2.2	1001	16	2	450	350
3.3	1010	16	3	475	325
4.4	1011	16	4	500	300
6.0	1100	15	5	500	250
8.0	1101	14	6	500	200
10.5	1110	13	7	500	150
14.0	1111	12	8	500	100

**Negative preemphasis levels denote deemphasis.*

Table 6. Serial Output Spread

SS	SPREAD (%)
000	No spread spectrum. **Power-up default when SSEN = low.**
001	±0.5% spread spectrum. **Power-up default when SSEN = high.**
010	±1.5% spread spectrum.
011	±2% spread spectrum.
100	No spread spectrum.
101	±1% spread spectrum.
110	±3% spread spectrum.
111	±4% spread spectrum.

Table 7. Spread-Spectrum Rate Limitations

3-CHANNEL MODE RXCLKIN_ FREQUENCY (MHz)	4-CHANNEL MODE RXCLKIN_ FREQUENCY (MHz)	SERIAL LINK BIT-RATE (Mbps)	AVAILABLE SPREAD RATES
< 33.3	< 25	< 1000	All rates available
33.3 to < 66.7	20 to <50	1000 to < 2000	1.5%, 1%, 0.5%
66.7+	50+	2000+	0.5%

Manual Programming of the Spread-Spectrum Divider

The modulation rate for the serializer relates to the RXCLKIN_ frequency as follows:

$$f_M = (1 + DRS)\frac{f_{RXCLKIN\_}}{MOD \times SDIV}$$

where:

f_M = Modulation frequency

DRS = DRS pin input value (0 or 1)

$f_{RXCLKIN\_}$ = RXCLKIN_ frequency

MOD = Modulation coefficient given in Table 8

SDIV = 6-bit SDIV setting, manually programmed by the µC

To program the SDIV setting, first look up the modulation coefficient according to the part number and desired bus-width and spread-spectrum settings. Solve the above equation for SDIV using the desired pixel clock and modulation frequencies. If the calculated SDIV value is larger than the maximum allowed SDIV value in Table 8, set SDIV to the maximum value.

Sleep Mode

The serializer includes a low-power sleep mode to reduce power consumption. Set the SLEEP bit to 1 to initiate sleep mode. The serializer sleeps immediately after setting its SLEEP = 1. See the *Link Startup Procedure* section for details on waking up the device for different µC and starting conditions.

The µC can only put the remote-side device to sleep. Use the $\overline{PWDN}$ input pin to bring the µC-side device into a low-power state. Entering sleep mode resets the HDCP registers but not the configuration registers.

Power-Down Mode

The serializer includes a shutdown mode to further reduce power consumption. Set $\overline{PWDN}$ low to enter power-down mode. While in power-down mode, the outputs of the device remain high impedance. Entering power-down mode resets the internal registers of the device. In addition, upon exiting power-down mode, the serializer relatches the state of SSEN, DRS, $\overline{AUTOS}$, and ADD_.

Configuration Link Mode

The GMSL includes a low-speed configuration link to allow control-data connection between the two devices in the absence of a valid clock input. In either display or camera applications, the configuration link can be used to program equalizer/preemphasis or other registers before establishing the video link. An internal oscillator provides RXCLKIN_ for establishing the serial configuration link between the serializer and GMSL deserializer. Set CLINKEN = 1 on the serializer to turn on the configuration link. The configuration link remains active as long as the video link has not been enabled. The video link overrides the configuration link and attempts to lock when SEREN = 1.

Link Startup Procedure

Table 9 lists four startup cases for video-display applications. Table 10 lists two startup cases for image-sensing applications. In either video-display or image-sensing applications, the control link is always available after the high-speed data link or the configuration link is

Table 8. Modulation Coefficients and Maximum SDIV Settings

BIT-WIDTH MODE	SPREAD-SPECTRUM SETTING (%)	MODULATION COEFFICIENT MOD (decimal)	SDIV UPPER LIMIT (decimal)
4-Channel	1	104	40
	0.5	104	63
	3	152	27
	1.5	152	54
	4	204	15
	2	204	30
3-Channel	1	80	52
	0.5	80	63
	3	112	37
	1.5	112	63
	4	152	21
	2	152	42

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established and the serializer/GMSL deserializer registers or the peripherals are ready for programming.

Video-Display Applications

For the video-display application with a remote display unit, connect the µC to the serializer and set CDS = low for both the serializer and GMSL deserializer. Table 9 summarizes the four startup cases based on the settings of $\overline{AUTOS}$ and MS.

Case 1: Autostart Mode

After power-up or when $\overline{PWDN}$ transitions from low to high for both the serializer and GMSL deserializer, the serial link establishes if a stable clock is present. The serializer locks to the clock and sends the serial data to the GMSL deserializer. The GMSL deserializer then detects activity on the serial link and locks to the input serial data.

Case 2: Standby Start Mode

After power-up or when $\overline{PWDN}$ transitions from low to high for both the serializer and GMSL deserializer, the GMSL deserializer starts up in sleep mode and the serializer stays in standby mode (does not send serial data). Use the µC and program the serializer to set SEREN = 1 to establish a video link, or CLINKEN = 1 to establish the configuration link. After locking to a stable clock (for SEREN = 1) or the internal oscillator (for CLINKEN = 1), the serializer sends a wake-up signal to the GMSL deserializer. The GMSL deserializer exits sleep mode after locking to the serial data and sets SLEEP = 0. If after 8ms the GMSL deserializer does not lock to the input serial data, the GMSL deserializer goes back to sleep and the internal sleep bit remains set (SLEEP = 1).

Case 3: Remote-Side Autostart Mode

After power-up or when $\overline{PWDN}$ transitions from low to high, the remote device (GMSL deserializer) starts up and tries to lock to an incoming serial signal with sufficient power. The host side (serializer) is in standby mode and does not try to establish a link. Use the µC and program the serializer to set SEREN = 1 (and apply a stable clock signal) to establish a video link, or CLINKEN = 1 to establish the configuration link. In this case, the GMSL deserializer ignores the short wake-up signal sent from the serializer.

Case 4: Remote Side in Sleep Mode

After power-up or when $\overline{PWDN}$ transitions from low to high, the remote device (GMSL deserializer) starts up in sleep mode. The high-speed link establishes automatically after the serializer powers up with a stable clock signal and sends a wake-up signal to the GMSL deserializer. Use this mode in applications where the GMSL deserializer powers up before the serializer.

Table 9. Start Mode Selection for Display Applications (CDS = Low)

CASE	$\overline{AUTOS}$ (SERIALIZER)	SERIALIZER POWER-UP STATE	MS (GMSL DESERIALIZER)	GMSL DESERIALIZER POWER-UP STATE	LINK STARTUP MODE
1	Low	Serialization enabled	Low	Normal (SLEEP = 0)	Both devices power up with serial link active (autostart).
2	High	Serialization disabled	High	Sleep mode (SLEEP = 1)	The serial link is disabled and the GMSL deserializer powers up in sleep mode. Set SEREN = 1 or CLINKEN = 1 in the serializer to start the serial link and wake up the GMSL deserializer.
3	High	Serialization disabled	Low	Normal (SLEEP = 0)	Both devices power up in normal mode with the serial link disabled. Set SEREN = 1 or CLINKEN = 1 in the serializer to start the serial link.
4	Low	Serialization enabled	High	Sleep mode (SLEEP = 1)	The GMSL deserializer starts in sleep mode. Link autostarts upon serializer power-up. Use this case when the GMSL deserializer powers up before the serializer.

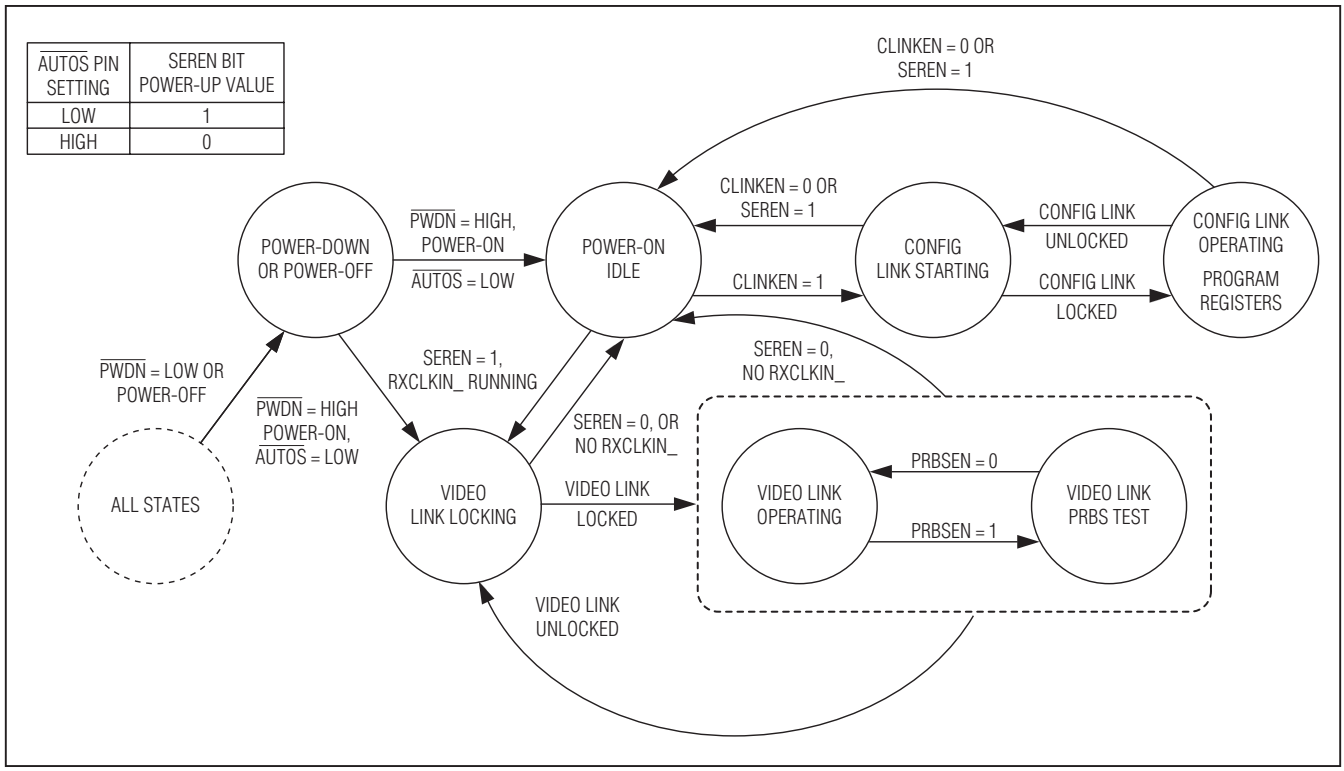

Figure 23. State Diagram, CDS = Low (LCD Application)

Image-Sensing Applications

For image-sensing applications, connect the µC to the GMSL deserializer and set CDS = high for both the serializer and GMSL deserializer. The GMSL deserializer powers up normally (SLEEP = 0) and continuously tries to lock to a valid serial input. Table 10 summarizes both startup cases, based on the state of the serializer's $\overline{AUTOS}$ pin.

Case 1: Autostart Mode

After power-up, or when $\overline{PWDN}$ transitions from low to high, the serializer locks to a stable input clock and sends the high-speed data to the GMSL deserializer. The GMSL deserializer locks to the serial data and outputs the video data and clock.

Case 2: Sleep Mode

After power-up or when $\overline{PWDN}$ transitions from low to high, the serializer starts up in sleep mode. To wake up the serializer, use the µC to send a GMSL-protocol UART frame containing at least three rising edges (e.g., 0x66), at a bit rate no greater than 1Mbps. The low-power wake-up receiver of the serializer detects the wake-up frame over the reverse control channel and powers up. Reset the sleep bit (SLEEP = 0) of the serializer using a regular control-channel write packet to power up the device fully. Send the sleep bit write packet at least 500µs after the wake-up frame. The serializer goes back to sleep mode if its sleep bit is not cleared within 5ms (min) after detecting a wake-up frame.

HDCP

The explanation of HDCP operation in this data sheet is given as a guide for general understanding. Implementation of HDCP in a product must meet the requirements given in the "HDCP System v1.3 Amendment for GMSL," which is available from DCP, LLC.

HDCP uses two main phases of operation: authentication and the link integrity check. The µC starts authentication by writing to the START_AUTHENTICATION bit in the serializer. The serializer generates a 64-bit random number. The host µC first reads the 64-bit random number from the serializer and writes it to the GMSL deserializer. The µC then reads the serializer public key selection vector (AKSV) and writes it to the GMSL deserializer. The µC then reads the GMSL deserializer KSV (AKSV)

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Table 10. Start Mode Selection for Image-Sensing Applications (CDS = High)

CASE	$\overline{\text{AUTOS}}$ (SERIALIZER)	SERIALIZER POWER-UP STATE	GMSL DESERIALIZER POWER-UP STATE	LINK STARTUP MODE
1	Low	Serialization enabled	Normal (SLEEP = 0)	Autostart.
2	High	Sleep mode (SLEEP = 1)	Normal (SLEEP = 0)	The serializer is in sleep mode. Wake up the serializer through the control channel (µC attached to GMSL deserializer).

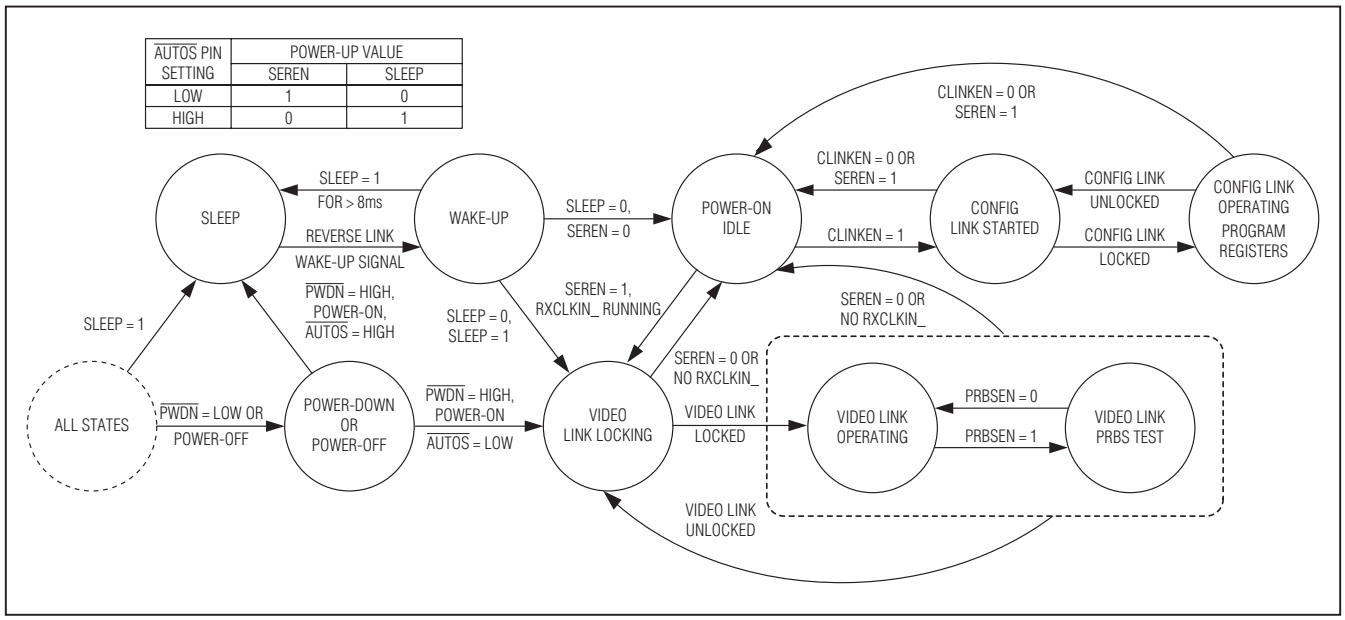

Figure 24. State Diagram, CDS = High (Camera Application)

and writes it to the serializer. The µC begins checking the receiver BKSV against the revocation list. Using the cipher, the serializer and GMSL deserializer calculate a 16-bit response value (R0 and R0', respectively). The GMSL amendment for HDCP reduces the 100ms minimum wait time allowed the receiver to generate R0' (specified in HDCP rev 1.3) to 128 pixel clock cycles in the GMSL amendment.

There are two response value comparison modes: internal comparison and µC comparison. Set EN_INT_COMP = 1 to select internal comparison mode. Set EN_INT_COMP = 0 to select µC comparison mode. In internal comparison mode, the µC reads the GMSL deserializer response R0' and writes it to the serializer. The serializer compares R0' to its internally generated response value R0, and sets R0_RI_MATCHED. In µC comparison mode, the µC reads and compares the R0/R0' values from the serializer/GMSL deserializer.

During response value generation and checking, the host µC checks for a valid BKSV against the revocation list. If BKSV is not on the list and the response values match, the host authenticates the link. If the response values do not match, the µC resamples the response values (as described in HDCP rev 1.3 Appendix C). If resampling fails, the µC restarts authentication. If BKSV appears on the revocation list, the host cannot transmit data that requires protection. The host knows when the link is authenticated and decides when to output data requiring protection. The µC performs a link integrity check every 128 frames or every 2s ±0.5s. The serializer/GMSL deserializer generate response values every 128 frames. These values are compared internally (internal comparison mode) or can be compared in the host µC.

In addition, the serializer/GMSL deserializer provide response values for the enhanced link verification feature. Enhanced link verification is an optional method of link verification for faster detection of loss-of-synchronization. For this option, the serializer and GMSL deserializer generate 16-bit values (Pj and Pj') every 16 frames. The host must detect three consecutive Pj/Pj' mismatches before going to the resampling.

Encryption Enable

The GMSL link transfers either encrypted or nonencrypted data. For encrypted data, the host µC sets the encryption enable (ENCRYPTION_ENABLE) bit in both the serializer and GMSL deserializer. The µC must set ENCRYPTION_ENABLE in the same VSYNC cycle in both the serializer and GMSL deserializer (no VSYNC falling edges between the two writes). The same timing applies when clearing ENCRYPTION_ENABLE to disable encryption.

Note: ENCRYPTION_ENABLE enables/disables encryption on the GMSL irrespective of the content. To comply with HDCP, the µC must not allow content requiring encryption to cross the GMSL unencrypted. See the *Force Video/Force Audio for Unencrypted Data* section.

The µC must complete the authentication process before enabling encryption. In addition, encryption must be disabled before starting a new authentication session.

VSYNC Detection

If the µC cannot detect the video vertical sync (VSYNC) falling edge, it can use the serializer's VSYNC_DET register bit. The host µC first writes 0 to the VSYNC_DET bit. The serializer then sets VSYNC_DET = 1 once it detects an internal VSYNC falling edge (which may correspond to an external VSYNC rising edge if INVVSYNC of the serializer is set). The µC continuously reads VSYNC_DET and waits for the next internal VSYNC falling edge before setting ENCRYPTION_ENABLE. Poll VSYNC_DET fast enough to allow time to set ENCRYPTION_ENABLE in both the serializer/GMSL deserializer within the same VSYNC cycle.

Synchronization of Encryption

The VSYNC synchronizes the start of encryption. Once encryption has started, the GMSL generates a new encryption key for each frame and each line, with the internal falling edge of VSYNC and HSYNC. Rekeying is transparent to data and does not disrupt the encryption of video or audio data.

Repeater Support

The serializer has features to build an HDCP repeater. An HDCP repeater receives and decrypts HDCP content and then encrypts and transmits on one or more downstream links. A repeater can also use decrypted HDCP content (e.g., to display on a screen). To support HDCP repeater authentication protocol, the GMSL deserializer has a REPEATER register bit. This register bit must be set to 1 by the µC (most likely on repeater module). Both the serializer and GMSL deserializer use SHA-1 hash-value calculation over the assembled KSV lists. HDCP GMSL links support a maximum of 15 receivers (total number including the ones in repeater modules). If the total number of receiver devices exceed 14, the µC must set the MAX_DEVS_EXCEEDED register bit when it assembles the KSV list.

Force Video/Force Audio for Unencrypted Data

The serializer masks audio and video data through two control bits: FORCE_AUDIO and FORCE_VIDEO. Set FORCE_VIDEO = 1 to transmit the 24-bit data word in the DFORCE register instead of the video data received at the LVDS input. Set FORCE_AUDIO = 0 to transmit 0 instead of the SD input (SCK and WS continue to be output from the deserializer). Use these features to blank out the screen and mute the audio.

_HDCP Authentication Procedures

The serializer generates a 64-bit random number exceeding the HDCP requirement. The serializer/GMSL deserializer internal one-time programmable (OTP) memories contain unique HDCP keyset programmed at the factory. The host µC initiates and controls the HDCP authentication procedure. The serializer and GMSL deserializer generate HDCP authentication response values for the verification of authentication. Use the following procedures to authenticate the HDCP GMSL encryption (refer to the *HDCP 1.3 Amendment for GMSL* for details). The µC must perform link integrity checks while encryption is enabled (see Tables 12 and 13). Any event that indicates that the GMSL deserializer has lost link synchronization should retrigger authentication. The µC must first write 1 to the RESET_HDCP bit in the serializer before starting a new authentication attempt.

HDCP Protocol Summary

Tables 11, 12, and 13 list the summaries of the HDCP protocol. These tables serve as an implementation guide only. Meet the requirements in the GMSL amendment for HDCP to be in full compliance.

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Table 11. Startup, HDCP Authentication and Normal Operation (GMSL DESERIALIZER is not a Repeater)—First Part of the HDCP Authentication Protocol

NO.	µC	SERIALIZER	GMSL DESERIALIZER
1	Initial state after power-up.	Powers up waiting for HDCP authentication.	Powers up waiting for HDCP authentication.
2	Ensures that A/V data not requiring protection (low-value content) is available at the serializer inputs (such as blue or informative screen). Alternatively, use the FORCE_VIDEO and FORCE_AUDIO bits of the serializer to mask the A/V data at the input of the serializer. Starts the link by writing SEREN = H or link starts automatically if $\overline{AUTOS}$ is low.	—	—
3	—	Starts serialization and transmits low-value content A/V data.	Locks to incoming data stream and outputs low-value content A/V data.
4	Reads the locked bit of the GMSL deserializer and makes sure link is established.	—	—
5	Optionally writes a random-number seed to the serializer.	Combines seed with internally generated random number. If no seed is provided, only internal random number is used.	—
6	If HDCP encryption is required, starts authentication by writing 1 to the START_AUTHENTICATION bit of the serializer.	Generates (stores) AN and resets the START_AUTHENTICATION bit to 0.	—
7	Reads AN and AKSV from the serializer and writes to the GMSL deserializer.	—	Generates R0' triggered by the µC's write of AKSV.
8	Reads the BKSV and REPEATER bit from the GMSL deserializer and writes to the serializer.	Generates R0, triggered by the µC's write of BKSV.	—
9	Reads the INVALID_BKSV bit of the serializer and continues with authentication if it is 0. Authentication can be restarted if it fails (set RESET_HDCP = 1 before restarting authentication).	—	—
10	Reads R0' from the GMSL deserializer and reads R0 from the serializer. If they match, continues with authentication; otherwise retries up to two more times (optionally, the serializer comparison can be used to detect if R0/R0' match). Authentication can be restarted if it fails (set RESET_HDCP = 1 before restarting authentication).	—	—
11	Waits for the VSYNC falling edge (internal to the serializer) and then sets the ENCRYPTION_ENABLE bit to 1 in the GMSL deserializer and serializer (if the µC is not able to monitor VSYNC, it can utilize the VSYNC_DET bit in the serializer).	Encryption is enabled after the next VSYNC falling edge.	Decryption is enabled after the next VSYNC falling edge.

Table 11. Startup, HDCP Authentication and Normal Operation (GMSL DESERIALIZER is not a Repeater)—First Part of the HDCP Authentication Protocol (continued)

NO.	µC	SERIALIZER	GMSL DESERIALIZER
12	Checks that BKSV is not in the Key Revocation List and continues if it is not. Authentication can be restarted if it fails. **Note:** Revocation list check can start after BKSV is read in step 8.	—	—
13	Starts transmission of the A/V content that needs protection.	Performs HDCP encryption on high-value content A/V data.	Performs HDCP decryption on high-value content A/V data.

Table 12. Link Integrity Check (Normal)—Performed Every 128 Frames After Encryption is Enabled

NO.	µC	SERIALIZER	GMSL DESERIALIZER
1	—	Generates Ri and updates the RI register every 128 VSYNC cycles.	Generates Ri' and updates the RI' register every 128 VSYNC cycles.
2	—	Continues to encrypt and transmit A/V data.	Continues to receive, decrypt, and output A/V data.
3	Every 128 video frames (VSYNC cycles) or every 2s.	—	—
4	Reads RI from the serializer.	—	—
5	Reads RI' from the GMSL deserializer.	—	—
6	Reads RI again from the serializer and ensures it is stable (matches the previous RI that it has read from the serializer). If RI is not stable, go back to step 5.	—	—
7	If RI matches RI', the link integrity check is successful; go back to step 3.	—	—
8	If RI does not match RI', the link integrity check fails. After the detection of failure of link integrity check, the µC ensures that A/V data not requiring protection (low-value content) is available at the serializer's inputs (such as blue or informative screen). Alternatively, the FORCE_VIDEO and FORCE_AUDIO bits of the serializer can be used to mask the A/V data input of the serializer.	—	—
9	Writes 0 to the ENCRYPTION_ENABLE bit of the serializer and GMSL deserializer.	Disables encryption and transmits low-value content A/V data.	Disables decryption and outputs low-value content A/V data.
10	Restarts authentication by writing 1 to the RESET_HDCP bit, followed by writing 1 to the START_AUTHENTICATION bit in the serializer.	—	—

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Table 13. Optional Enhanced Link Integrity Check—Performed Every 16 Frames After Encryption is Enabled

NO.	µC	SERIALIZER	GMSL DESERIALIZER
1	—	Generates Pj and updates the PJ register every 16 VSYNC cycles.	Generates Pj' and updates the PJ' register every 16 VSYNC cycles.
2	—	Continues to encrypt and transmit the A/V data.	Continues to receive, decrypt, and output the A/V data.
3	Every 16 video frames: reads PJ from the serializer and PJ' from the GMSL deserializer.	—	—
4	If PJ matches PJ', enhanced link integrity check is successful; go back to step 3.	—	—
5	If there is a mismatch, retry up to two more times from step 3. Enhanced link integrity check fails after three mismatches. After the detection of failure of enhanced link integrity check, the µC ensures that A/V data not requiring protection (low-value content) is available at the serializer inputs (such as blue or informative screen). Alternatively, the FORCE_VIDEO and FORCE_AUDIO bits of the serializer can be used to mask the A/V data input of the serializer.	—	—
6	Writes 0 to the ENCRYPTION_ENABLE bit of the serializer and GMSL deserializer.	Disables encryption and transmits low-value content A/V data.	Disables decryption and outputs low-value content A/V data.
7	Restarts authentication by writing 1 to the RESET_HDCP bit, followed by writing 1 to the START_AUTHENTICATION bit in the serializer.	—	—

Example Repeater Network—Two µCs

The example shown in Figure 25 has one repeater and two µCs. Table 14 summarizes the authentication operation.

Detection and Action Upon New Device Connection

When a new device is connected to the system, the device must be authenticated and the device's KSV is checked against the revocation list. The downstream µCs can set the NEW_DEV_CONN bit of the upstream receiver and invoke an interrupt to notify upstream µCs.

Notification of Start of Authentication and Enable of Encryption to Downstream Links

HDCP repeaters do not immediately begin authentication upon startup or detection of a new device, but instead wait for an authentication request from the upstream transmitter/repeaters.

Use the following procedure to notify downstream links of the start of a new authentication request:

1) Host µC begins authentication with HDCP repeater's input receiver.
2) When AKSV is written to HDCP repeater's input receiver, its AUTH_STARTED bit is automatically set and its GPIO1 goes high (if GPIO1_FUNCTION is set to high).
3) HDCP repeater's µC waits for a low-to-high transition on HDCP repeater input receiver's AUTH_STARTED bit and/or GPIO1 (if configured) and starts authentication downstream.
4) HDCP repeater's µC resets AUTH_STARTED bit.

Set GPIO0_FUNCTION to high to have GPIO0 follow the ENCRYPTION_ENABLE bit of the receiver. The repeater µC can use this function to be notified when encryption is enabled/disabled by an upstream µC.

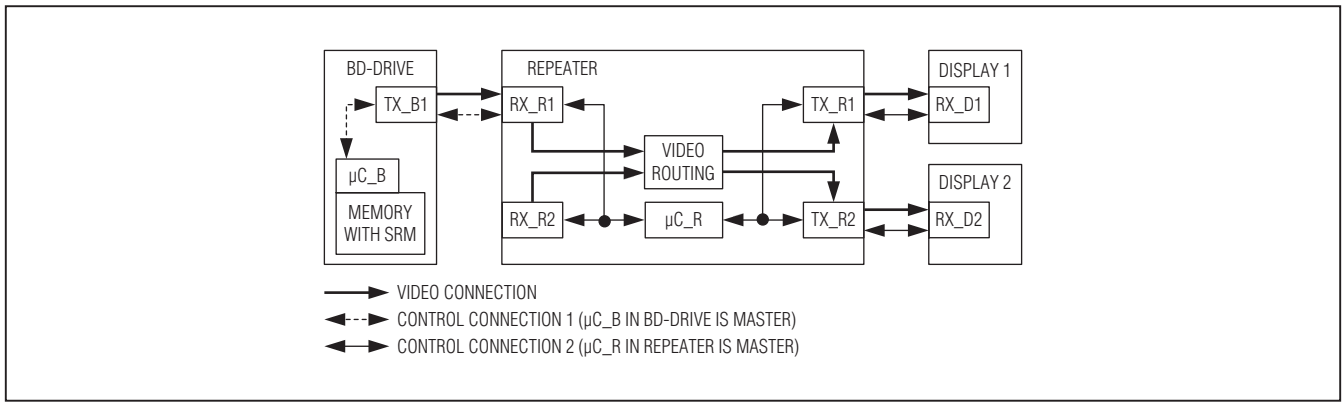

Figure 25. Example Network with One Repeater and Two µCs (TXs are for the Serializer and RXs are for the GMSL Deserializer)

Table 14. HDCP Authenticaion and Normal Operation (One Repeater, Two µCs)—First and Second Parts of the HDCP Authentication Protocol

NO.	µC_B	µC_R	SERIALIZER (TX_B1, TX_R1, TX_R2)	GMSL DESERIALIZER (RX_R1, RX_D1, RX_D2)
—	—	—	TX_B1 CDS = 0 TX_R1 CDS = 0 TX_R2 CDS = 0	RX_R1 CDS = 1 RX_D1 CDS = 0 RX_D2 CDS = 0
1	Initial state after power-up.	Initial state after power-up.	All: Power-up waiting for HDCP authentication.	All: Power-up waiting for HDCP authentication.
2	—	Writes REPEATER = 1 in RX_R1. Retries until a proper acknowledge frame is received. **Note:** This step must be completed before the first part of the authentication is started between TX_B1 and RX_R1 by µC_B (step 7). For example, to satisfy this requirement, RX_R1 can be held at power-down until µC_R is ready to write the REPEATER bit. Alternatively, µC_B can poll µC_R before starting authentication.	—	—

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Table 14. HDCP Authenticaion and Normal Operation (One Repeater, Two µCs)—First and Second Parts of the HDCP Authentication Protocol (continued)

NO.	µC_B	µC_R	SERIALIZER (TX_B1, TX_R1, TX_R2)	GMSL DESERIALIZER (RX_R1, RX_D1, RX_D2)
3	Ensures that the A/V data not requiring protection (low-value content) is available at TX_B1 inputs (such as blue or informative screen). Alternatively, the FORCE_VIDEO and FORCE_AUDIO bits of TX_B1 can be used to mask the A/V data input of TX_B1. Starts the link between TX_B1 and RX_R1 by writing SEREN = H to TX_B1 or link starts automatically if $\overline{AUTOS}$ is low.	—	TX_B1: Starts serialization and transmits low-value content A/V data.	RX_R1: Locks to incoming data stream and outputs low-value content A/V data.
4	—	Starts all downstream links by writing SEREN = H to TX_R1, TX_R2, or links start automatically if $\overline{AUTOS}$ of the transmitters are low.	TX_R1, TX_R2: Starts serialization and transmits low-value content A/V data.	RX_D1, RX_D2: Locks to incoming data stream and outputs low-value content A/V data.
5	Reads the locked bit of RX_R1 and ensures link between TX_B1 and RX_R1 is established.	Reads the locked bit of RX_D1 and ensures link between TX_R1 and RX_D1 is established. Reads the locked bit of RX_D2 and ensures link between TX_R2 and RX_D2 is established.	—	—
6	Optionally, writes a random-number seed to TX_B1.	Writes 1 to the GPIO_0_FUNCTION and GPIO_1_FUNCTION bits in RX_R1 to change GPIO functionality to be used for HDCP purpose. Optionally, writes a random-number seed to TX_R1 and TX_R2.	—	—
7	Starts and completes first part of the authentication protocol between TX_B1, RX_R1 (see steps 6–10 in Table 11).	—	TX_B1: According to the commands from µC_B, generates AN, computes R0.	RX_R1: According to the commands from µC_B, computes R0'.
8	—	When GPIO_1 = 1 is detected, starts and completes first part of the authentication protocol between (TX_R1, RX_D1) and (TX_R2, RX_D2) links (see steps 6–10 in Table 11).	TX_R1, TX_R2: According to the commands from µC_R, generates AN, computes R0.	RX_D1, RX_D2: According to the commands from µC_R, computes R0'.

Table 14. HDCP Authenticaion and Normal Operation (One Repeater, Two µCs)—First and Second Parts of the HDCP Authentication Protocol (continued)

NO.	µC_B	µC_R	SERIALIZER (TX_B1, TX_R1, TX_R2)	GMSL DESERIALIZER (RX_R1, RX_D1, RX_D2)
9	Waits for the VSYNC falling edge and then enables encryption on the (TX_B1, RX_R1) link. Full authentication is not complete yet so it ensures A/V content that needs protection is not transmitted. Since REPEATER = 1 was read from RX_R1, the second part of authentication is required.	—	TX_B1: Encryption is enabled after the next VSYNC falling edge.	RX_R1: Decryption is enabled after the next VSYNC falling edge.
10	—	When GPIO_0 = 1 is detected, enables encryption on the (TX_R1, RX_D1) and (TX_R2, RX_D2) links.	TX_R1, TX_R2: Encryption is enabled after the next VSYNC falling edge.	RX_D1, RX_D2: Decryption is enabled after the next VSYNC falling edge.
11	Waits for some time to allow µC_R to make the KSV List ready in RX_R1. Then polls (reads) the KSV_LIST_READY bit of RX_R1 regularly until the proper acknowledge frame is received and bit is read as 1.	Blocks control channel from µC_B side by setting REVCCEN = FWDCCEN = 0 in RX_R1. Retries until the proper acknowledge frame is received.	—	RX_R1: Control channel from the serializer side (TX_B1) is blocked after FWDCCEN = REVCCEN = 0 is written.
12		Writes BKSVs of RX_D1 and RX_D2 to KSV List in RX_R1. Then calculates and writes BINFO register of RX_R1.	—	RX_R1: Triggered by µC_R's write of BINFO, calculates hash value (V') on the KSV list, BINFO, and the secret value M0'.
13		Writes 1 to the KSV_LIST_READY bit of RX_R1 and then unblocks control channel from µC_B side by setting REVCCEN = FWDCCEN = 1 in RX_R1.	—	RX_R1: Control channel from the serializer side (TX_B1) is unblocked after FWDCCEN = REVCCEN = 1 is written.

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Table 14. HDCP Authenticaion and Normal Operation (One Repeater, Two µCs)—First and Second Parts of the HDCP Authentication Protocol (continued)

NO.	µC_B	µC_R	SERIALIZER (TX_B1, TX_R1, TX_R2)	GMSL DESERIALIZER (RX_R1, RX_D1, RX_D2)
14	Reads the KSV List and BINFO from RX_R1 and writes them to TX_B1. If any of the MAX_DEVS_EXCEEDED or MAX_CASCADE_EXCEEDED bits is 1, then authentication fails. **Note:** BINFO must be written after the KSV List.	—	TX_B1: Triggered by µC_B's write of BINFO, calculates hash value (V) on the KSV list, BINFO, and the secret value M0.	—
15	Reads V from TX_B1 and V' from RX_R1. If they match, continues with authentication; otherwise, retries up to two more times.	—	—	—
16	Searches for each KSV in the KSV List and BKSV of RX_R1 in the Key Revocation List.	—	—	—
17	If keys are not revoked, second part of authentication protocol is completed.	—	—	—
18	Starts transmission of the A/V content that needs protection.	—	All: Perform HDCP encryption on high-value A/V data.	All: Perform HDCP decryption on high-value A/V data.

Applications Information

Self PRBS Test

The serializer/GMSL deserializer link includes a PRBS pattern generator and bit-error verification function. First, disable the glitch filters (set DISVSFILT, DISHSFILT to 1) in the GMSL deserializer. Next, disable VSYNC/HSYNC inversion in both the serializer and GMSL deserialzer (set INVVSYNC, INVHSYNC to 0). Then, set PRBSEN = 1 (0x04, D5) in the serializer and then the GMSL deserializer to start the PRBS test. Set PRBSEN = 0 (0x04, D5) first in the GMSL deserializer and then the serializer to exit the PRBS self test.

Microcontrollers on Both Sides of the GMSL Link (Dual µC Control)

Usually the microcontroller is either on the serializer side for video-display applications or on the GMSL deserializer side for image-sensing applications. For the former case, both the CDS pins of the serializer/GMSL deserializer are set to low, and for the later case, the CDS pins are set to high. However, if the CDS pin of the serializer is low and the same pin of the GMSL deserializer is high, then the serializer/GMSL deserializer connect to both µCs simultaneously. In such a case, the µCs on either side can communicate with the serializer and GMSL. Contentions of the control link can happen if the µCs on both sides are using the link at the same time. The serializer/GMSL deserializer do not provide the solution for contention avoidance. The serializer/GMSL deserializer do not send an acknowledge frame when communication fails due to contention. Users can always implement a higher layer protocol to avoid the contention. In addition, if UART communication across the serial link is not required, the µCs can disable the forward and reverse control channel through the FWDCCEN and REVCCEN bits (0x04, D[1:0]) in the serializer/GMSL deserializer. UART communication across the serial link is stopped and contention between µCs no longer occurs. During dual µC operation, if one of the CDS pins on either side changes state, the link resumes the corresponding state described in the *Link Startup Procedure* section.

As an example of dual µC use in an image-sensing application, the serializer can be in sleep mode and waiting for wake-up by the GMSL deserializer. After wake-up, the serializer-side µC sets the serializer's CDS pin low and assumes master control of the serializer's registers.

Jitter-Filtering PLL

In some applications, the LVDS input clock to the serializer (RXCLKIN_) includes noise, which reduces link reliability. The serializer has a narrowband jitter-filtering PLL to attenuate frequency components outside the PLL's bandwidth (< 100kHz, typ). Enable the jitter-filtering PLL by setting DISFPLL = 0 (0x05, D6).

Changing the Clock Frequency

Both the video clock rate ($f_{RXCLKIN\_}$) and the control-channel clock rate (f_{UART}) can be changed on-the-fly to support applications with multiple clock speeds. It is recommended to enable the serial link after the video clock stabilizes. To recalibrate any automatic settings if a clean frequency change cannot be guaranteed, stop the video clock for 5µs and restart the serial link or toggle SEREN after each change in the video clock frequency. The reverse control channel remains unavailable for 350µs after serial link start or stop. Limit on-the-fly changes in f_{UART} to factors of less than 3.5 at a time to ensure that the device recognizes the UART sync pattern. For example, when lowering the UART frequency from 1Mbps to 100kbps, first send data at 333kbps and then at 100kbps to have reduction ratios of 3 and 3.333, respectively.

Do not interrupt RXCLKIN or change its frequency while encryption is enabled. Otherwise HDCP synchronization is lost and authentication must be repeated. To change the RXCLKIN_ frequency, stop the high-value content A/V data. Then disable encryption in the serializer/GMSL deserializer within the same VSYNC cycle—encryption stops at the next VSYNC falling edge. RXCLKIN can now be changed/stopped. Reenable encryption before sending any high-value content A/V data.

Fast Detection of Loss-of-Synchronization

A measure of link quality is the recovery time from loss of HDCP synchronization. With the GMSL, loss of GMSL lock usually accompanies a loss of HDCP sync. The host can be quickly notified of loss-of-lock by connecting the GMSL deserializer LOCK output to the INT input. If other sources use the interrupt input, such as a touch-screen controller, the µC can implement a routine to distinguish between interrupts from loss-of-sync and normal interrupts. Reverse control-channel communication does not require an active forward link to operate and accurately tracks the LOCK status of the video link. LOCK asserts for video link only and not for the configuration link.

Software Programming of the Device Addresses

Both the serializer and GMSL deserializer have software-programmable device addresses. This allows multiple GMSL devices, along with I²C peripherals to coexist on the same control channel. The serializer device address is stored in registers 0x00 of each device, while the deserializer device address is stored in register 0x01 of each device. To change the device address, first write to the device whose address changes (register 0x00 of the serializer for serializer device address change, or register 0x01 of the GMSL deserializer for deserializer device address change). Then write the same address into the corresponding register on the other device (register 0x00 of the GMSL deserializer for serializer device address change, or register 0x01 of the serializer for deserializer device address change).

3-Level Inputs for Default Device Address

ADD0 and ADD1 are 3-level inputs that control the serializer's default device slave addresses (Table 2). Connect ADD0/ADD1 through a pullup resistor to IOVDD, a pulldown resistor to GND, or a high-impedance connection. For digital control, use three-state logic to drive the 3-level logic inputs.

ADD0/ADD1 set the device addresses in the serializer only and not the GMSL deserializer. Set the GMSL deserializer's ADD0/ADD1 inputs to the same settings as the serializer. Alternatively, write to register 0x00 and 0x01 of the GMSL deserializer to reflect any changes made due to the 3-level inputs.

Configuration Blocking

The serializer can block changes to its non-HDCP registers. Set CFGBLOCK to make all non-HDCP registers as read only. Once set, the registers remain blocked until the supplies are removed or until $\overline{PWDN}$ is low.

Backward Compatibility

The serializer is backward compatible with the non-HDCP MAX9249 serializer, with the following exceptions:

- **Address pins:** The ADD0 and ADD1 pins on the serializer are the reserved pins on the MAX9249 serializer. Connect ADD0 and ADD1 to GND to set the serializer's default device addresses to the same values as the MAX9249 serializer.

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- **First UART packet delay:** The µC must wait 2.7ms after power-up before sending the first UART packet to the serializer. This delay is < 200µs for the MAX9249 serializer.

The pinouts and packages are otherwise the same for both devices. See Table 3 and the *Pin Description* for backward-compatible pin mapping.

Key Memory

Each device has a unique HDCP key set that is stored in secure on-chip nonvolatile memory (NVM). The HDCP key set consists of forty 56-bit private keys and one 40-bit public key. The NVM is qualified for automotive applications.

Line-Fault Detection

The line-fault detector in the serializer monitors for line failures such as short to ground, short to battery, and open link for system fault diagnosis. Figure 3 shows the required external resistor connections. $\overline{LFLT}$ = low when a line fault is detected and $\overline{LFLT}$ goes high when the line returns to normal. The line-fault type is stored in 0x08 D[3:0] of the serializer. Filter $\overline{LFLT}$ with the µC to reduce the detector's susceptibility to short ground shifts. The fault detector threshold voltages are referenced to the serializer ground. Additional passive components set the DC level of the cable (Figure 3). If the serializer and GMSL deserializer grounds are different, the link DC voltage during normal operation can vary and cross one of the fault-detection thresholds. For the fault-detection circuit, select the resistor's power rating to handle a short to the battery.

To detect the short-together case, refer to Application Note 4709: *GMSL Line-Fault Detection*.

Table 15 lists the mapping for line-fault types.

Internal Input Pulldowns

The control and configuration inputs on the serializer/GMSL deserializer include a pulldown resistor to GND. Pulldowns are disabled when the device is shut down ($\overline{PWDN}$ = low) or put into sleep mode. Keep all inputs driven or use external pullup/pulldown resistors to prevent additional current consumption and undesired configuration due to undefined inputs.

Choosing I²C/UART Pullup Resistors

Both I²C/UART open-drain lines require pullup resistors to provide a logic-high level. There are tradeoffs between power dissipation and speed, and a compromise made in choosing pullup resistor values. Every device connected to the bus introduces some capacitance even when the device is not in operation. I²C specifies 300ns rise times to go from low to high (30% to 70%) for fast mode, which is defined for data rates up to 400kbps (see the I²C specifications in the *Electrical Characteristics* table for details). To meet the fast-mode rise-time requirement, choose the pullup resistors so that rise time t_R = 0.85 x R_{PULLUP} x C_{BUS} < 300ns. The waveforms are not recognized if the transition time becomes too slow. The serializer/GMSL deserializer supports I²C/UART rates up to 1Mbps.

AC-Coupling

AC-coupling isolates the receiver from DC voltages up to the voltage rating of the capacitor. Four capacitors (two at the serializer output and two at the deserializer input) are needed for proper link operation and to provide protection if either end of the cable is shorted to a high voltage. AC-coupling blocks low-frequency ground shifts and low-frequency common-mode noise.

Table 15. Line-Fault Mapping

REGISTER ADDRESS	BITS	NAME	VALUE	LINE FAULT TYPE
0x08	D[3:2]	LFNEG	00	Negative cable wire shorted to supply voltage.
			01	Negative cable wire shorted to ground.
			10	Normal operation.
			11	Negative cable wire disconnected.
	D[1:0]	LFPOS	00	Positive cable wire shorted to supply voltage.
			01	Positive cable wire shorted to ground.
			10	Normal operation.
			11	Positive cable wire disconnected.

**For the short-together case, refer to* Application Note 4709: GMSL Line-Fault Detection.

Selection of AC-Coupling Capacitors

Voltage droop and the digital sum variation (DSV) of transmitted symbols cause signal transitions to start from different voltage levels. Because the transition time is finite, starting the signal transition from different voltage levels causes timing jitter. Choose the time constant for an AC-coupled link to reduce droop and jitter to an acceptable level. The RC network for an AC-coupled link consists of the CML receiver termination resistor (R_{TR}), the CML driver termination resistor (R_{TD}), and the series AC-coupling capacitors (C). The RC time constant for four equal-value series capacitors is (C x (R_{TD} + R_{TR}))/4. R_{TD} and R_{TR} are required to match the transmission line impedance (usually 100Ω). This leaves the capacitor selection to change the system time constant. Use at least 0.2µF high-frequency surface-mount ceramic capacitors, with sufficient voltage rating to withstand a short to battery, to pass the lower speed reverse control-channel signal. Use capacitors with a case size less than 3.2mm x 1.6mm to have lower parasitic effects to the high-speed signal.

Power-Supply Circuits and Bypassing

The serializer uses an AVDD and DVDD of 1.7V to 1.9V, and an LVDSVDD of 3.0V to 3.6V. All single-ended inputs and outputs derive power from an IOVDD of 1.7V to 3.6V, which scale with IOVDD. Proper voltage-supply bypassing is essential for high-frequency circuit stability.

Cables and Connectors

Interconnect for CML typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Twisted-pair and shielded twisted-pair cables tend to generate less EMI due to magnetic-field canceling effects. Balanced cables pick up noise as common mode rejected by the CML receiver. Table 16 lists the suggested cables and connectors used in the GMSL link.

Board Layout

Separate the digital signals and CML/LVDS high-speed signals to prevent crosstalk. Use a four-layer PCB with separate layers for power, ground, CML/LVDS, and digital signals. Lay out PCB traces close to each other for a 100Ω differential characteristic impedance. The trace dimensions depend on the type of trace used (microstrip or stripline). Note that two 50Ω PCB traces do not have 100Ω differential impedance when brought close together—the impedance goes down when the traces are brought closer.

Route the PCB traces for a CML/LVDS channel (there are two conductors per CML/LVDS channel) in parallel to maintain the differential characteristic impedance. Avoid vias. Keep PCB traces that make up a differential pair equal length to avoid skew within the differential pair.

ESD Protection

The serializer's ESD tolerance is rated for Human Body Model, IEC 61000-4-2, and ISO 10605. The ISO 10605 and IEC 61000-4-2 standards specify ESD tolerance for electronic systems. CML/LVDS I/O are tested for ISO 10605 ESD protection and IEC 61000-4-2 ESD protection. All pins are tested for the Human Body Model. The Human Body Model discharge components are C_S = 100pF and R_D = 1.5kΩ (Figure 26). The IEC 61000-4-2 discharge components are C_S = 150pF and R_D = 330Ω (Figure 27). The ISO 10605 discharge components are C_S = 330pF and R_D = 2kΩ (Figure 28).

Table 16. Suggested Connectors and Cables for GMSL

VENDOR	CONNECTOR	CABLE
Rosenberger	D4S10A-40ML5-Z	Dacar 538
Nissei	GT11L-2S	F-2WME AWG28
JAE	MX38-FF	A-BW-Lxxxxx

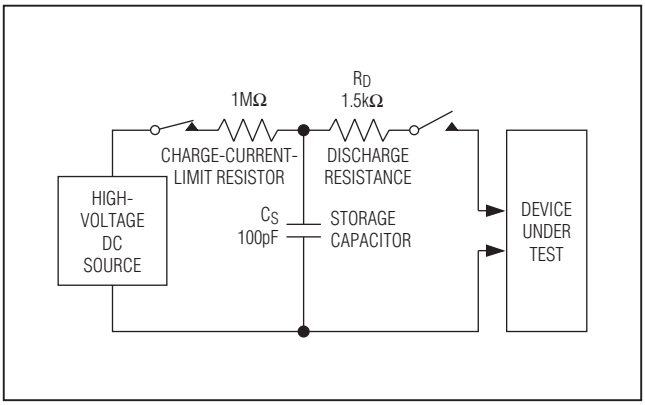

Figure 26. Human Body Model ESD Test Circuit

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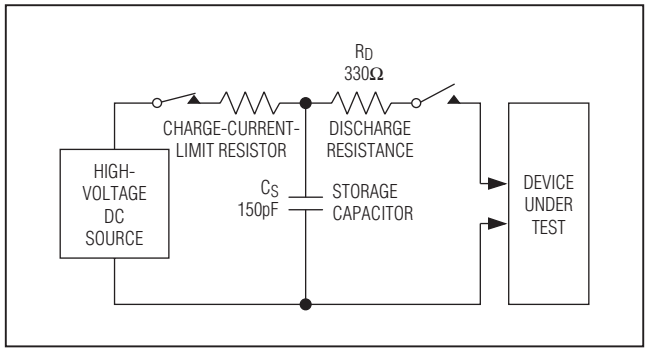

Figure 27. IEC 61000-4-2 Contact Discharge ESD Test Circuit

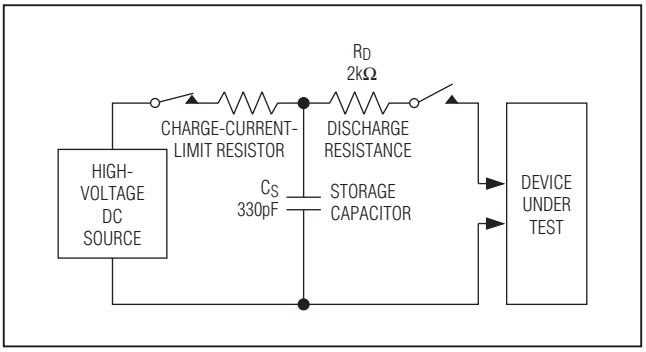

Figure 28. ISO 10605 Contact Discharge ESD Test Circuit

Table 17. Serializer GMSL Core Register Table (see Table 1)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x00	D[7:1]	SERID	XXXXXXX	Serializer device address. Power-up default address determined by ADD0 and ADD1 (see Table 2).	XX00XX0
	D0	CFGBLOCK	0	Normal operation.	0
			1	Registers 0x00 to 0x1F are read only.	
0x01	D[7:1]	DESID	XXXXXXX	Deserializer device address. Power-up default address determined by ADD0 and ADD1 (see Table 2).	XX01XX0
	D0	—	0	Reserved.	0
0x02	D[7:5]	SS	**000**	No spread spectrum. **Power-up default when SSEN = low.**	000, 001
			001	±0.5% spread spectrum. **Power-up default when SSEN = high.**	
			010	±1.5% spread spectrum.	
			011	±2% spread spectrum.	
			100	No spread spectrum.	
			101	±1% spread spectrum.	
			110	±3% spread spectrum.	
			111	±4% spread spectrum.	
	D4	AUDIOEN	0	Disable I²S channel.	1
			1	Enable I²S channel.	
	D[3:2]	PRNG	00	12.5MHz to 25MHz pixel clock.	11
			01	25MHz to 50MHz pixel clock.	
			10	50MHz to 104MHz pixel clock.	
			11	Automatically detect the pixel clock range.	
	D[1:0]	SRNG	00	0.5Gbps to 1Gbps serial-bit rate.	11
			01	1Gbps to 2Gps serial-bit rate.	
			10	2Gbps to 3.125Gbps serial-bit rate.	
			11	Automatically detect serial-bit rate.	

Table 17. Serializer GMSL Core Register Table (see Table 1) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x03	D[7:6]	AUTOFM	00	Calibrate spread-modulation rate only once after locking.	00
			01	Calibrate spread-modulation rate every 2ms after locking.	
			10	Calibrate spread-modulation rate every 16ms after locking.	
			11	Calibrate spread-modulation rate every 256ms after locking.	
	D[5:0]	SDIV	000000	Autocalibrate sawtooth divider.	000000
			XXXXXX	Manual SDIV setting. See the *Manual Programming of the Spread-Spectrum Divider* section.	
0x04	D7	SEREN	**0**	Disable serial link. **Power-up default when $\overline{\text{AUTOS}}$ = high.** Reverse control-channel communication remains unavailable for 350µs after the serializer starts/stops the serial link.	0, 1
			1	Enable serial link. **Power-up default when $\overline{\text{AUTOS}}$ = low.** Reverse control-channel communication remains unavailable for 350µs after the serializer starts/stops the serial link.	
	D6	CLINKEN	0	Disable configuration link.	0
			1	Enable configuration link.	
	D5	PRBSEN	0	Disable PRBS test.	0
			1	Enable PRBS test.	
	D4	SLEEP	0	Normal mode. Default value depends on the CDS and $\overline{\text{AUTOS}}$ pin values at power-up).	0, 1
			1	Activate sleep mode. Default value depends on the CDS and $\overline{\text{AUTOS}}$ pin values at power-up.	
	D[3:2]	INTTYPE	00	Base mode uses I²C peripheral interface.	00
			01	Base mode uses UART peripheral interface.	
			10, 11	Base mode peripheral interface disabled.	
	D1	REVCCEN	0	Disable reverse control channel from deserializer (receiving).	1
			1	Enable reverse control channel from deserializer (receiving).	
	D0	FWDCCEN	0	Disable forward control channel to deserializer (sending).	1
			1	Enable forward control channel to deserializer (sending).	

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Table 17. Serializer GMSL Core Register Table (see Table 1) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x05	D7	I2CMETHOD	0	I²C conversion sends the register address.	0
			1	Disable sending of I²C register address (command-byte-only mode).	
	D6	DISFPLL	0	Filter PLL active.	1
			1	Filter PLL disabled.	
	D[5:4]	CMLLVL	00	Do not use.	11
			01	200mV CML signal level.	
			10	300mV CML signal level.	
			11	400mV CML signal level.	
	D[3:0]	PREEMP	0000	Preemphasis off.	0000
			0001	-1.2dB preemphasis.	
			0010	-2.5dB preemphasis.	
			0011	-4.1dB preemphasis.	
			0100	-6.0dB preemphasis.	
			0101	Do not use.	
			0110	Do not use.	
			0111	Do not use.	
			1000	1.1dB preemphasis.	
			1001	2.2dB preemphasis.	
			1010	3.3dB preemphasis.	
			1011	4.4dB preemphasis.	
			1100	6.0dB preemphasis.	
			1101	8.0dB preemphasis.	
			1110	10.5dB preemphasis.	
			1111	14.0dB preemphasis.	
0x06	D[7:0]	—	01000000	Reserved.	01000000
0x07	D[7:0]	—	00100010	Reserved.	00100010
0x08	D[7:4]	—	0000	Reserved.	0000 (read only)
	D[3:2]	LFNEG	00	Negative cable wire shorted to supply voltage.	10 (read only)
			01	Negative cable wire shorted to ground.	
			10	Normal operation.	
			11	Negative cable wire disconnected.	
	D[1:0]	LFPOS	00	Positive cable wire shorted to supply voltage.	10 (read only)
			01	Positive cable wire shorted to ground.	
			10	Normal operation.	
			11	Positive cable wire disconnected.	
0x0C	D[7:0]	—	01110000	Reserved.	01110000

Table 17. Serializer GMSL Core Register Table (see Table 1) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x0D	D7	SETINT	0	Set INT low when SETINT transitions from 1 to 0.	0
			1	Set INT high when SETINT transitions from 0 to 1.	
	D6	INVVSYNC	0	Serializer does not invert VSYNC.	0
			1	Serializer inverts VSYNC.	
	D5	INVHSYNC	0	Serializer does not invert HSYNC.	0
			1	Serializer inverts HSYNC.	
	D[4:0]	—	00000	Reserved.	00000
	D4	DISRES	0	RES (LVDS interface) mapped to DIN27.	0
			1	CNTL1 mapped to DIN27.	
	D[3:0]	SKEWADJ	0000	Adjust x7PLL clock skew +50ps.	1111
			0001	Adjust x7PLL clock skew +100ps.	
			0010	Adjust x7PLL clock skew +200ps.	
			0011	Adjust x7PLL clock skew +250ps.	
			0100	Adjust x7PLL clock skew +300ps.	
			0101	Adjust x7PLL clock skew +350ps.	
			0110	Adjust x7PLL clock skew +400ps.	
			0111	Do not use.	
			1000	Adjust x7PLL clock skew +50ps.	
			1001	Adjust x7PLL clock skew +100ps.	
			1010	Adjust x7PLL clock skew +200ps.	
			1011	Adjust x7PLL clock skew +250ps.	
			1100	Adjust x7PLL clock skew +300ps.	
			1101	Adjust x7PLL clock skew +350ps.	
			1110	Adjust x7PLL clock skew +400ps.	
			1111	No x7PLL clock skew adjustment.	
0x1E	D[7:0]	ID	00000111	Device identifier (MAX9265 = 0x07).	00000111 (read only)
0x1F	D[7:5]	—	000	Reserved.	000 (read only)
	D4	CAPS	0	Not HDCP capable.	1 (read only)
			1	HDCP capable.	
	D[3:0]	REVISION	XXXX	Device revision.	(read only)

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Table 18. Serializer HDCP Register Table (see Table 1)

REGISTER ADDRESS	SIZE (BYTES)	NAME	READ/ WRITE	FUNCTION	DEFAULT VALUE (hex)
0x80 to 0x84	5	BKSV	Read/write	HDCP receiver KSV	0x0000000000
0x85 to 0x86	2	RI/RI'	Read/write	RI (read only) of the transmitter when EN_INT_COMP = 0 RI' (read/write) of the receiver when EN_INT_COMP = 1	0x0000
0x87	1	PJ/PJ'	Read/write	PJ (read only) of the transmitter when EN_INT_COMP = 0 PJ' (read/write) of the receiver when EN_INT_COMP = 1	0x00
0x88 to 0x8F	8	AN	Read only	Session random number	(Read only)
0x90 to 0x94	5	AKSV	Read only	HDCP transmitter KSV	(Read only)
0x95	1	ACTRL	Read/write	D7 = PD_HDCP 1 = Power down HDCP circuits 0 = HDCP circuits normal	0x00
				D6 = EN_INT_COMP 1 = Internal comparison mode 0 = µC comparison mode	
				D5 = FORCE_AUDIO 1 = Force audio data to 0 0 = Normal operation	
				D4 = FORCE_VIDEO 1 = Force video data DFORCE value 0 = Normal operation	
				D3 = RESET_HDCP 1 = Reset HDCP circuits Automatically set to 0 upon completion 0 = Normal operation	
				D2 = START_AUTHENTICATION 1 = Start authentication Automatically set to 0 once authentication starts 0 = Normal operation	
				D1 = VSYNC_DET 1 = Internal falling edge on VSYNC detected 0 = No falling edge detected	
				D0 = ENCRYPTION_ENABLE 1 = Enable encryption 0 = Disable encryption	

Table 18. Serializer HDCP Register Table (see Table 1) (continued)

REGISTER ADDRESS	SIZE (BYTES)	NAME	READ/ WRITE	FUNCTION	DEFAULT VALUE (hex)
0x96	1	ASTATUS	Read only	D[7:4] = Reserved	0x00 (read only)
				D3 = V_MATCHED 1 = V matches V' (when EN_INT_COMP = 1) 0 = V does not match V' or EN_INT_COMP = 0	
				D2 = PJ_MATCHED 1 = PJ matches PJ' (when EN_INT_COMP = 1) 0 = PJ does not match PJ' or EN_INT_COMP = 0	
				D1 = R0_RI_MATCHED 1 = RI matches RI' (when EN_INT_COMP = 1) 0 = RI does not match RI' or EN_INT_COMP = 0	
				D0 = BKSV_INVALID 1 = BKSV is not valid 0 = BKSV is valid	
0x97	1	BCAPS	Read/write	D[7:1] = RESERVED	0x00
				D0 = REPEATER 1 = Set to 1 if device is a repeater 0 = Set to 0 if device is not a repeater	
0x98 to 0x9C	5	ASEED	Read/write	Internal random number generator optional seed value	0x0000000000
0x9D to 0x9F	3	DFORCE	Read/write	Forced video data transmitted when FORCE_VIDEO = 1 R[7:0] = DFORCE[7:0] G[7:0] = DFORCE[15:8] B[7:0] = DFORCE[23:16]	0x000000
0xA0 to 0xA3	4	V.H0, V'.H0	Read/write	H0 part of SHA-1 hash value V (read only) of the transmitter when EN_INT_COMP = 0 V' (read/write) of the receiver when EN_INT_COMP = 1	0x00000000
0xA4 to 0xA7	4	V.H1, V'.H1	Read/write	H1 part of SHA-1 hash value V (read only) of the transmitter when EN_INT_COMP = 0 V' (read/write) of the receiver when EN_INT_COMP = 1	0x00000000
0xA8 to 0xAB	4	V.H2, V'.H2	Read/write	H2 part of SHA-1 hash value V (read only) of the transmitter when EN_INT_COMP = 0 V' (read/write) of the receiver when EN_INT_COMP = 1	0x00000000

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Table 18. Serializer HDCP Register Table (see Table 1) (continued)

REGISTER ADDRESS	SIZE (BYTES)	NAME	READ/ WRITE	FUNCTION	DEFAULT VALUE (hex)
0xAC to 0xAF	4	V.H3, V'.H3	Read/write	H3 part of SHA-1 hash value V (read only) of the transmitter when EN_INT_COMP = 0 V' (read/write) of the receiver when EN_INT_COMP = 1	0x00000000
0xB0 to 0xB3	4	V.H4, V'.H4	Read/write	H4 part of SHA-1 hash value V (read only) of the transmitter when EN_INT_COMP = 0 V' (read/write) of the receiver when EN_INT_COMP = 1	0x00000000
0xB4 to 0xB5	2	BINFO	Read/write	D[15:12] = Reserved	0x0000
				D11 = MAX_CASCADE_EXCEEDED 1 = Set to one if more than 7 cascaded devices attached 0 = Set to zero if 7 or fewer cascaded devices attached	
				D[10:8] = DEPTH Depth of cascaded devices	
				D7 = MAX_DEVS_EXCEEDED 1 = Set to one if more than 14 devices attached 0 = Set to zero if 14 or fewer devices attached	
				D[6:0] = DEVICE_COUNT Number of devices attached	
0xB6	1	GPMEM	Read/write	General-purpose memory byte	0x00
0xB7 to 0xB9	3	—	Read only	Reserved	0x000000
0xBA to 0xFF	70	KSV_LIST	Read/write	List of KSV's downstream repeaters and receivers (maximum of 14 devices)	All zero

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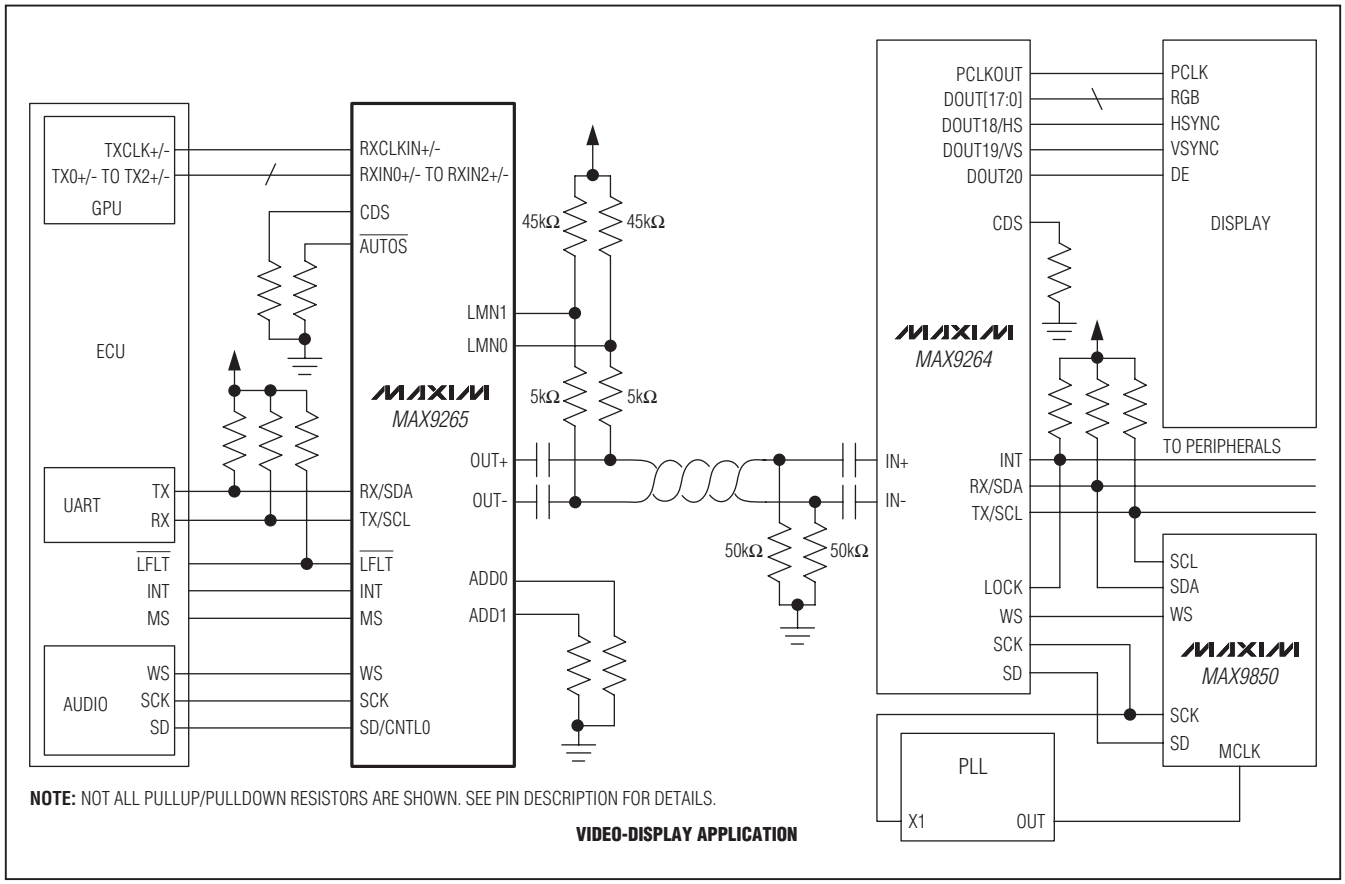
Typical Application Circuit



NOTE: NOT ALL PULLUP/PULLDOWN RESISTORS ARE SHOWN. SEE PIN DESCRIPTION FOR DETAILS.

VIDEO-DISPLAY APPLICATION

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 TQFP-EP	C48E+8	21-0065	90-0138

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/10	Initial release	—